

RELIABILITY REPORT
FOR
MAX3340EEUD
PLASTIC ENCAPSULATED DEVICES

May 24, 2002

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by



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Conclusion

The MAX3340E successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX3340E bidirectional level translator converts logic-level signals to USB signals, and USB signals to logic-level signals. It includes the 1.5k USB termination resistor internally, and supports both full-speed (12Mbps) and low-speed (1.5Mbps) USB operation. It has built-in $\pm 15\text{kV}$ ESD protection circuitry to guard the USB I/O pins, D+ and D-

The MAX3340E operates with V_L at voltages as low as 1.8V, ensuring compatibility with low-voltage ASICs. The MAX3340E features a logic selectable suspend mode that lowers current draw to less than 200 μA . The MAX3340E has a unique re-enumerate feature that allows changes in USB communication protocol while the power is on. The MAX3340E is fully compliant with USB specification 1.1, and the full-speed and low-speed operation under USB specification 2.0.

The MAX3340E is available in the miniature 4 x 4 chip-scale package, as well as the small 14-pin TSSOP, and is rated for the -40°C to $+85^\circ\text{C}$ extended temperature range.

B. Absolute Maximum Ratings

<u>Item</u>	<u>Rating</u>
VCC to GND	-0.3V to +6V
VL to GND	-0.3V to +5.5V
D+, D- to GND	-0.3V to (VTRM + 0.3V)
VP, VM, SUSP, OE/ENUMERATE, MODE, SPEED, RENB, RCV	-0.3V to (VL + 0.3V)
VTRM to GND	-0.3V to (VCC + 0.3V)
Maximum Continuous Output Current	$\pm 50\text{mA}$
Short-Circuit Duration (D+, D- to VCC or GND)	Continuous
Storage Temp.	-65°C to $+150^\circ\text{C}$
Junction Temperature	$+150^\circ\text{C}$
Lead Temp. (10 sec.)	$+300^\circ\text{C}$
Continuous Power Dissipation (TA = $+70^\circ\text{C}$)	
14-Lead TSSOP	727mW
Derates above $+70^\circ\text{C}$	
14-Lead TSSOP	9.1mW/ $^\circ\text{C}$

II. Manufacturing Information

- A. Description/Function: +/-15kV ESD-Protected USB Level Translator
- B. Process: SG1.2 (Standard 1.2 micron silicon gate CMOS)
- C. Number of Device Transistors: 981
- D. Fabrication Location: Oregon or California, USA
- E. Assembly Location: Philippines or Thailand
- F. Date of Initial Production: July, 2001

III. Packaging Information

- A. Package Type: **14-Lead TSSOP**
- B. Lead Frame: Copper
- C. Lead Finish: Solder Plate
- D. Die Attach: Silver-filled Epoxy
- E. Bondwire: Gold (1.0 mil dia.)
- F. Mold Material: Epoxy with silica filler
- G. Assembly Diagram: Buildsheet # 05-2601-0038
- H. Flammability Rating: Class UL94-V0
- I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112: Level 1

IV. Die Information

- A. Dimensions: 82 x 82 mils
- B. Passivation: $\text{Si}_3\text{N}_4/\text{SiO}_2$ (Silicon nitride/ Silicon dioxide)
- C. Interconnect: Aluminum/Si (Si = 1%)
- D. Backside Metallization: None
- E. Minimum Metal Width: 1.2 microns (as drawn)
- F. Minimum Metal Spacing: 1.2 microns (as drawn)
- G. Bondpad Dimensions: 5 mil. Sq.
- H. Isolation Dielectric: SiO_2
- I. Die Separation Method: Wafer Saw

V. Quality Assurance Information

- A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)
Bryan Preeshl (Executive Director)
Kenneth Huening (Vice President)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4389 \times 45 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

└ Temperature Acceleration factor assuming an activation energy of 0.8eV

$$\lambda = 24.13 \times 10^{-9}$$

$$\lambda = 24.13 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-5709) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The RT18 die type has been found to have all pins able to withstand a transient pulse of $\pm 1000\text{V}$, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of $\pm 150\text{mA}$.

Table 1
Reliability Evaluation Test Results

MAX3340EEUD

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		45	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 96hrs.	DC Parameters & functionality	TSSOP	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.

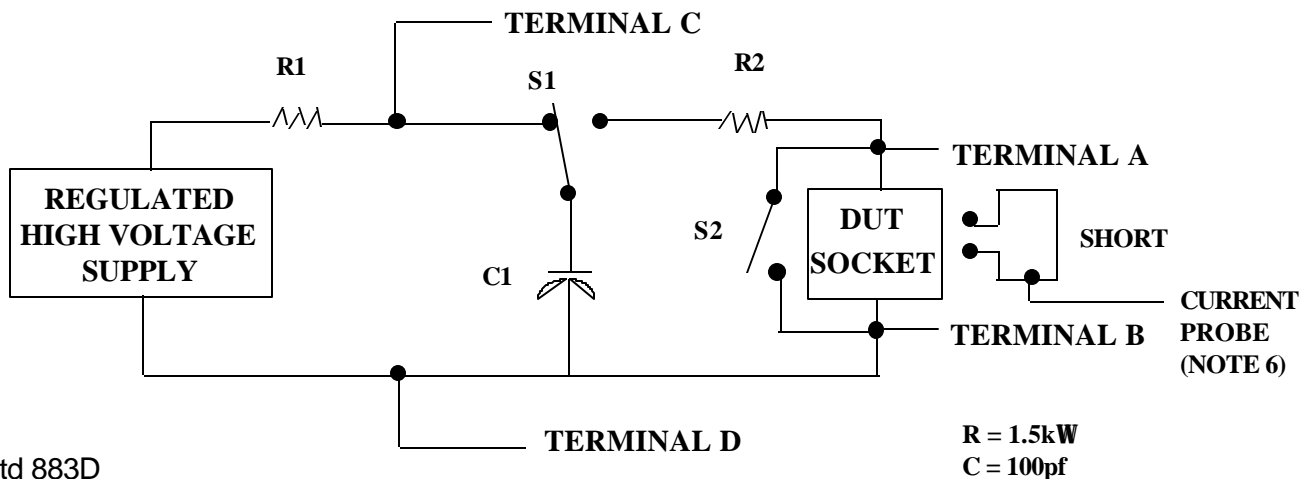
2/ No connects are not to be tested.

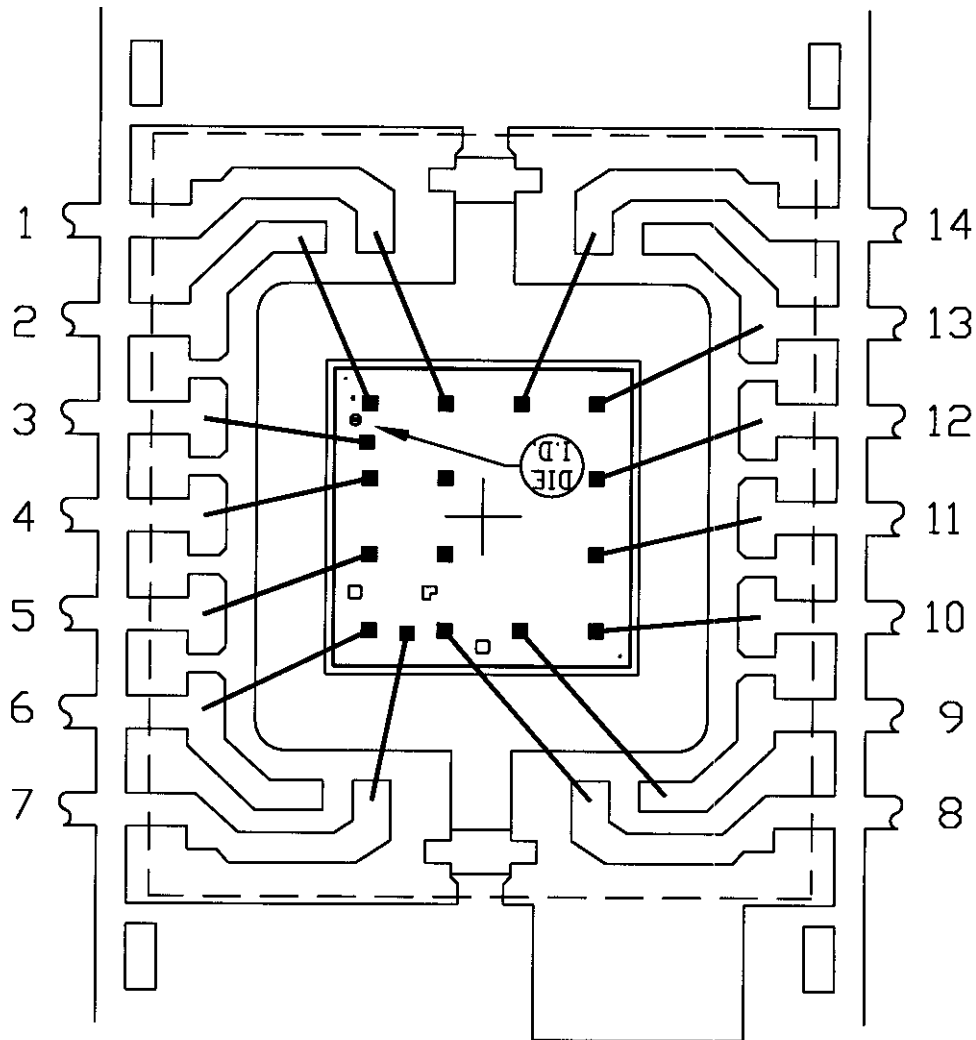
3/ Repeat pin combination I for each named Power supply and for ground

(e.g., where V_{PS1} is V_{DD} , V_{CC} , V_{SS} , V_{BB} , GND, $+V_S$, $-V_S$, V_{REF} , etc).

3.4 Pin combinations to be tested.

- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1} , or V_{SS2} or V_{SS3} or V_{CC1} , or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.





PKG. CODE: U14-1	
CAV./PAD SIZE: 118x122	PKG. DESIGN

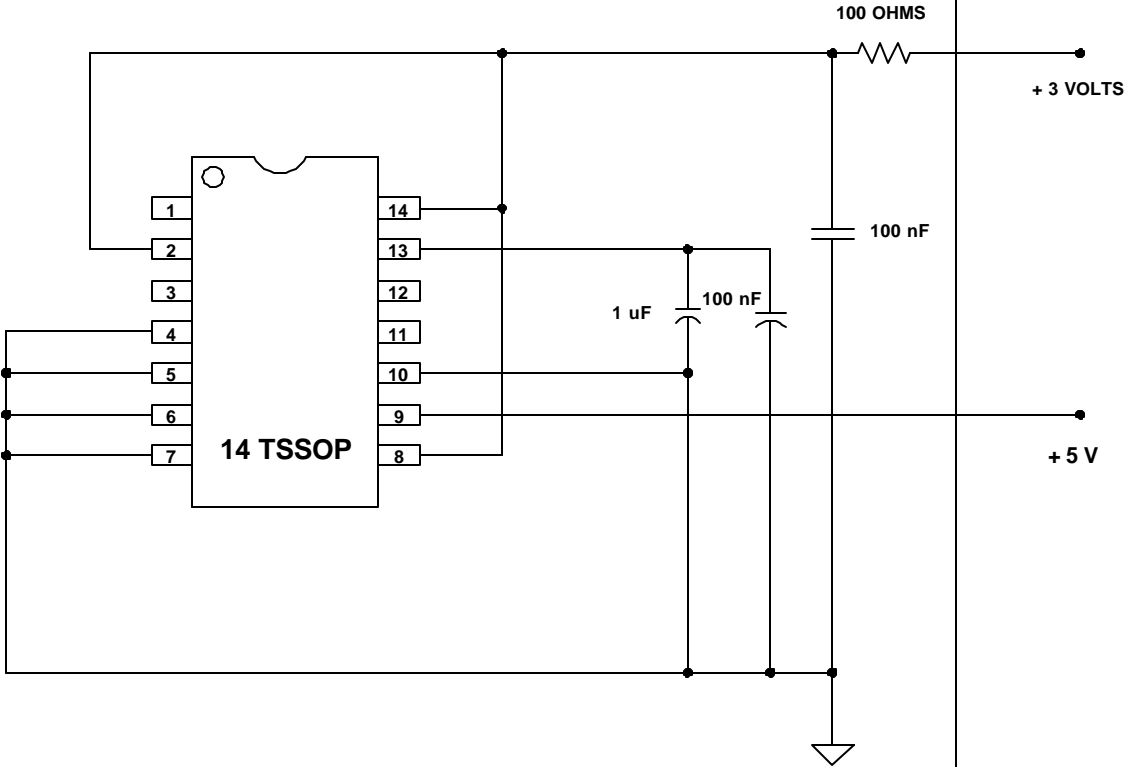
SIGNATURES

DATE

MAXIM CONFIDENTIAL & PROPRIETARY	
BOND DIAGRAM #: 05-2601-0038	REV: A

ONCE PER SOCKET

ONCE PER BOARD



DEVICES: MAX 3340 E

MAX. EXPECTED CURRENT = 5 mA; 20 mA (5V)

DRAWN BY:

NOTES: