

RELIABILITY REPORT
FOR
MAX3202EEWS+T
WAFER LEVEL PRODUCTS

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MAXIM INTEGRATED

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SAN JOSE, CA 95134

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Conclusion

The MAX3202EEWS+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX3202E/MAX3203E/MAX3204E/MAX3206E are low-capacitance $\pm 15\text{kV}$ ESD-protection diode arrays designed to protect sensitive electronics attached to communication lines. Each channel consists of a pair of diodes that steer ESD current pulses to VCC or GND. The MAX3202E/MAX3203E/MAX3204E/MAX3206E protect against ESD pulses up to $\pm 15\text{kV}$ Human Body Model, $\pm 8\text{kV}$ Contact Discharge, and $\pm 15\text{kV}$ Air-Gap Discharge, as specified in IEC 61000-4-2. These devices have a 5pF capacitance per channel, making them ideal for use on high-speed data I/O interfaces. The MAX3202E is a two-channel device intended for USB and USB 2.0 applications. The MAX3203E is a triple-ESD structure intended for USB On-the-Go (OTG) and video applications. The MAX3204E is a quad-ESD structure designed for Ethernet and FireWire® applications, and the MAX3206E is a six-channel device designed for cell phone connectors and SVGA video connections. All devices are available in tiny 4-bump (1.05mm x 1.05mm) WLP, 6-bump (1.05mm x 1.57mm) WLP, 9-bump (1.52mm x 1.52mm) WLP, 6-pin (3mm x 3mm) TDFN, and 12-pin (4mm x 4mm) TQFN packages and are specified for -40°C to $+85^{\circ}\text{C}$ operation.

II. Manufacturing Information

A. Description/Function:	Low-Capacitance, 2/3/4/6-Channel, ±15kV ESD-Protection Arrays for High-Speed Data Interfaces
B. Process:	BCD8
C. Number of Device Transistors:	
D. Fabrication Location:	Oregon
E. Assembly Location:	Japan
F. Date of Initial Production:	January 25, 2003

III. Packaging Information

A. Package Type:	4 bmp WLP
B. Lead Frame:	N/A
C. Lead Finish:	N/A
D. Die Attach:	None
E. Bondwire:	N/A
F. Mold Material:	N/A
G. Assembly Diagram:	#05-9000-3121
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	1
J. Single Layer Theta Ja:	N/A
K. Single Layer Theta Jc:	N/A
L. Multi Layer Theta Ja:	87°C/W
M. Multi Layer Theta Jc:	N/A

IV. Die Information

A. Dimensions:	44X44 mils
B. Passivation:	Si ₃ N ₄ /SiO ₂ (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	3.0 microns (as drawn)
F. Minimum Metal Spacing:	3.0 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO ₂
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

- A. Quality Assurance Contacts: Richard Aburano (Manager, Reliability Engineering)
Don Lipps (Manager, Reliability Engineering)
Bryan Preeshl (Vice President of QA)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% for all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 96 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 11.4 \times 10^{-9}$$

$$\lambda = 11.4 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at <http://www.maximintegrated.com/qa/reliability/monitor>. Cumulative monitor data for the BCD8 Process results in a FIT Rate of 0.14 @ 25C and 2.34 @ 55C (0.8 eV, 60% UCL).

B. E.S.D. and Latch-Up Testing (ESD lot ICA0AQ001D D/C 0239, Latch-Up lot NCA0BA005B D/C 0445)

The RT69 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2000V per Mil-Std 883 Method 3015.7. Latch-Up testing has shown that this device withstands a current of +/-250mA.

Table 1
Reliability Evaluation Test Results

MAX3202EEWS+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135°C	DC Parameters & functionality	48	0	NCA0BA005B, D/C 0445
	Biased		48	0	ICA0AQ001D, D/C 0239
	Time = 192 hrs.				

Note 1: Life Test Data may represent plastic DIP qualification lots.