RELIABILITY REPORT

FOR

MAX313LxxE

PLASTIC ENCAPSULATED DEVICES

April 8, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

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Conclusion

The MAX313L successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX313L analog switch features low on-resistance (10Ω max) and 1.5Ω on-resistance matching between channels. This switch is +3V logic compatible when powered from ±15V or +12V supplies. This switch conducts equally well in either direction. It offers low leakage over temperature (2.5nA at +85°C). Low power consumption and ESD tolerance greater than 2000V per Method 3015.7 are guaranteed.

The MAX313 is a quad, single-pole/single-throw (SPST) analog switch. The MAX313 is normally open (NO). This device operates from a single supply of +4.5V to +30V or from dual supplies of ±4.5V to ±20V.

B. Absolute Maximum Ratings

Item	Rating
(Voltages Referenced to GND)	
V+	-0.3V to +44V
V-	+0.3V to -44V
V+ to V-	-0.3V to +44V
VIN_ to V-	-0.3V to +44V
All Other Pins (Note 1)	(V- - 0.3V) to (V+ + 0.3V)
Continuous Current (COM_, NO_, NC_)	±100mA
Peak Current (COM_, NO_, NC_)	
(pulsed at 1ms, 10% duty cycle max)	±300mA
Operating Temperature Ranges	
MAX313LC_E	0°C to +70°C
MAX313LE_E	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C
Continuous Power Dissipation (TA = +70°C)	
16-Pin PDIP	842mW
16-Pin SO	696mW
16-Pin TSSOP	457mW
Derates above +70°C	
16-Pin PDIP	10.53mW/°C
16-Pin SO	8.7mW/°C
16-Pin TSSOP	6.7mW/°

Note 1: Signals on NC_, NO_, COM_, or IN_ exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current rating.

II. Manufacturing Information

A. Description/Function:	10Ω, Quad, SPST, CMOS Analog Switch
B. Process:	S5HV - Medium voltage 5 micron silicon gate CMOS
C. Number of Device Transistors:	92
D. Fabrication Location:	Oregon, USA
E. Assembly Location:	Philippines, Malaysia or Thailand
F. Date of Initial Production:	October, 2001

III. Packaging Information

A. Package Type:	**16 Lead TSSOP**	**16-Lead PDIP**	**16-Lead SO**
B. Lead Frame:	Copper	Copper	Copper
C. Lead Finish:	Solder Plate	Solder Plate	Solder Plate
D. Die Attach:	Silver-filled Epoxy	Silver-filled Epoxy	Silver-filled Epoxy
E. Bondwire:	Gold (1.0 mil dia.)	Gold (1.0 mil dia.)	Gold (1.0 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	# 05-1201-0254	# 05-1201-0252	# 05-1201-0253
H. Flammability Rating:	Class UL94-V0	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1	Level 1	Level 1

IV. Die Information

A. Dimensions:	85 x 140 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	5 microns (as drawn)
F. Minimum Metal Spacing:	5 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Manager, Reliability Operations)
Bryan Preeshl (Executive Director of QA)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 66 \times 2}$$

(Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 16.45 \times 10^{-9}$ $\lambda = 16.45$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The attached Burn-In Schematic (Spec. # 06-5002) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The AH78-1 die type has been found to have all pins able to withstand a transient pulse of ±400V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1
Reliability Evaluation Test Results

MAX313LxxE

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		66	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	NSO PDIP TSSOP	77 77 77	0 0 0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

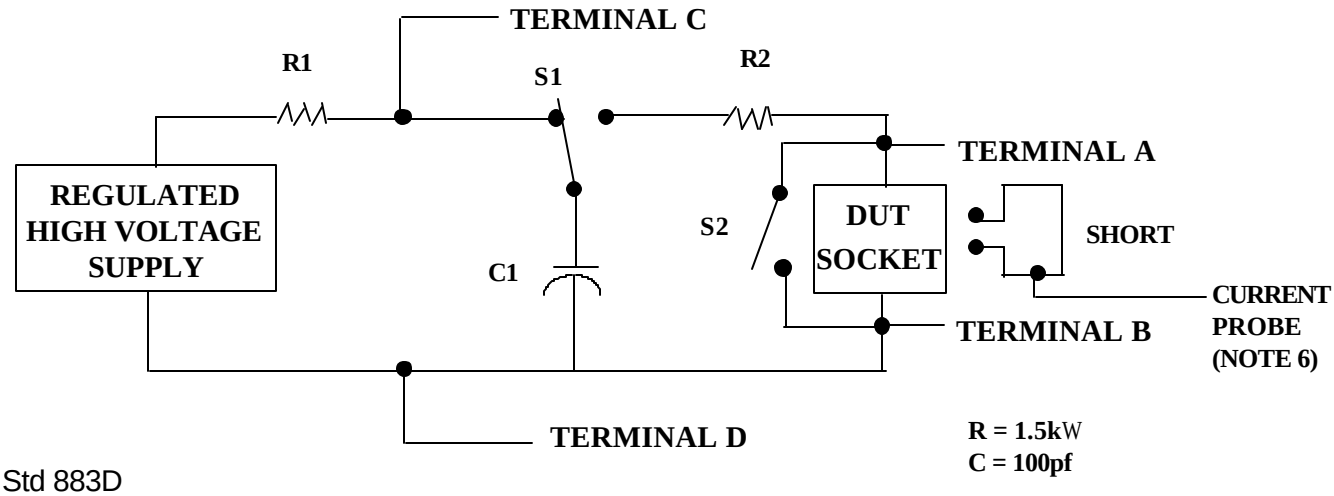
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

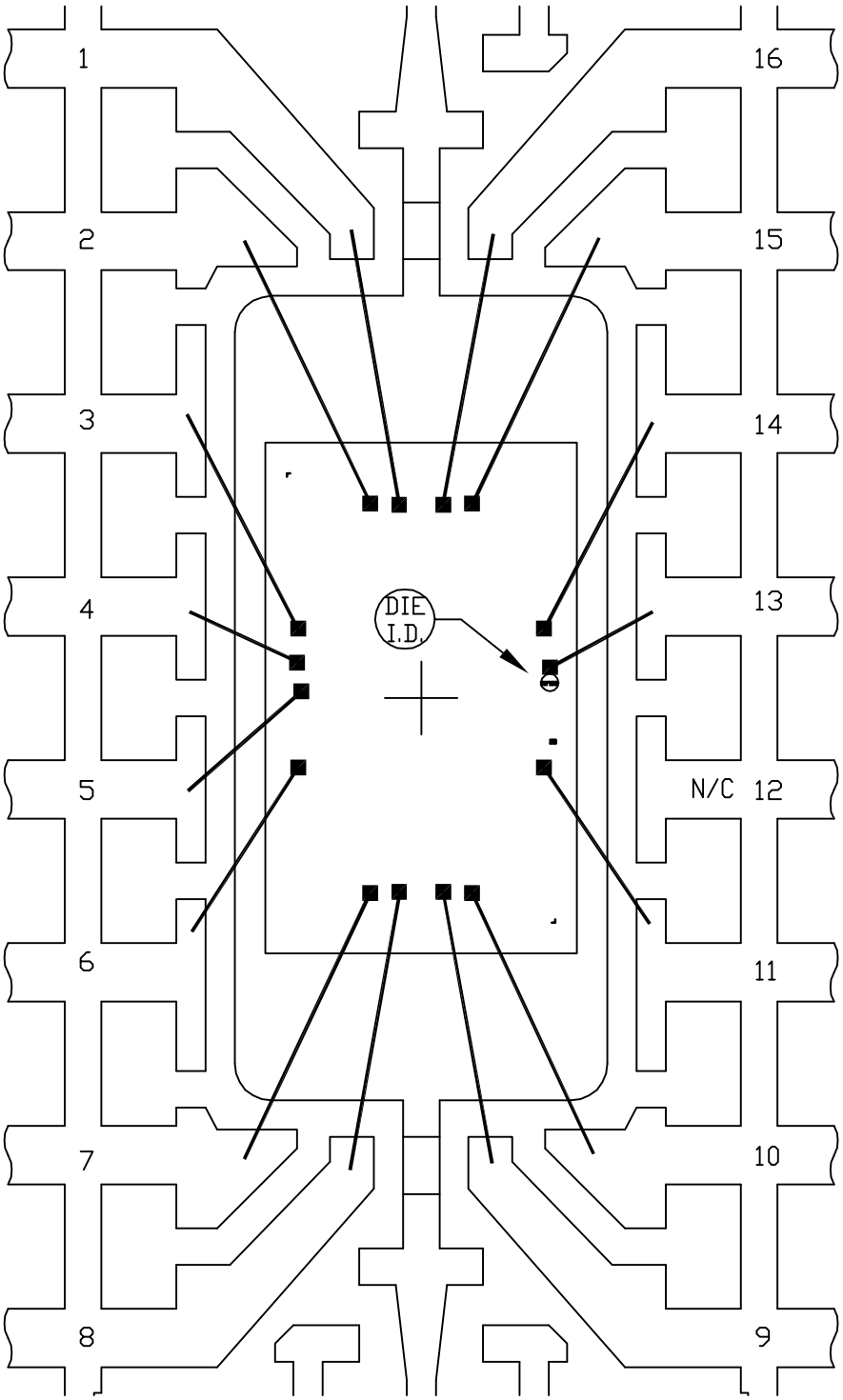
a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

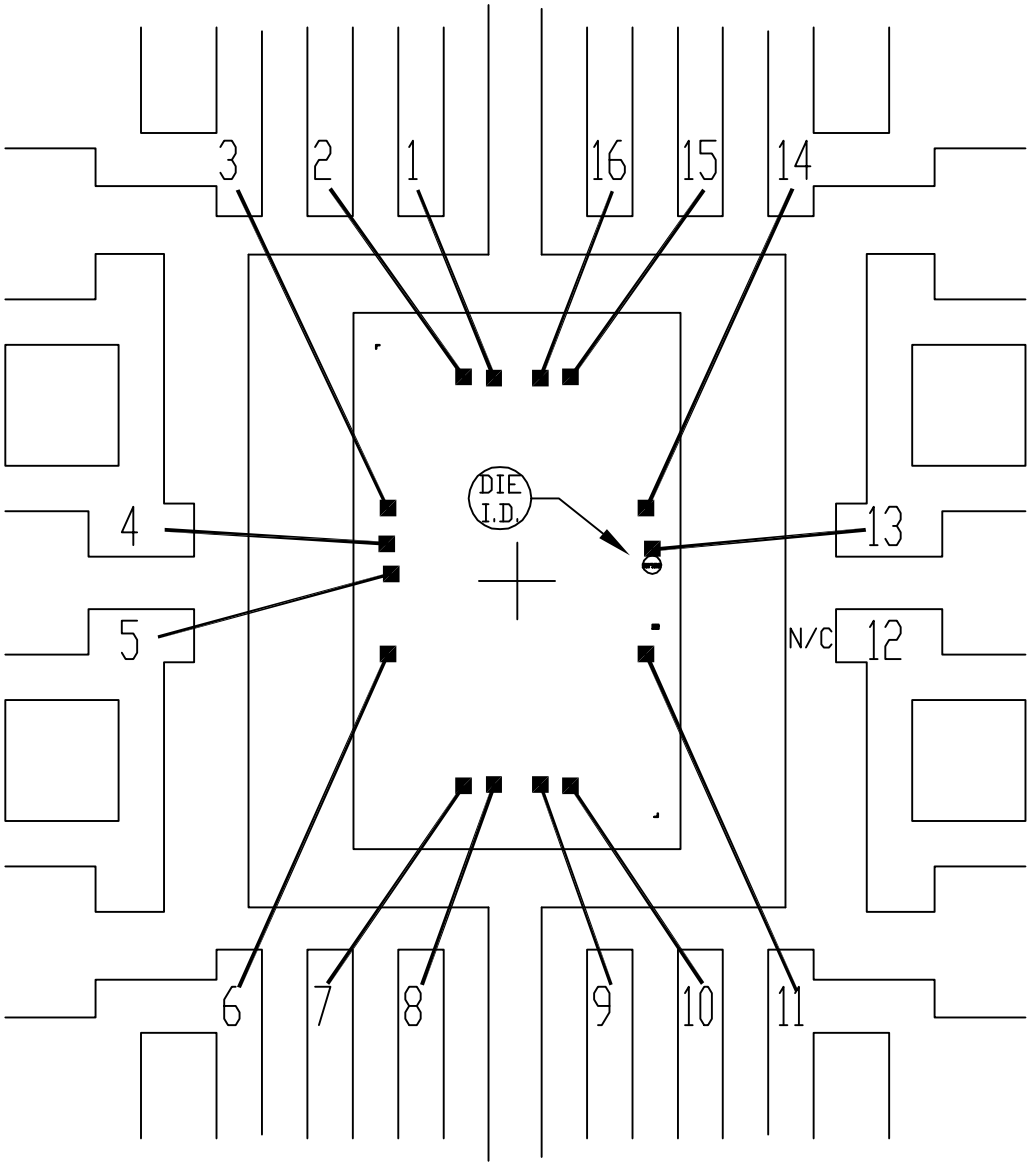
c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



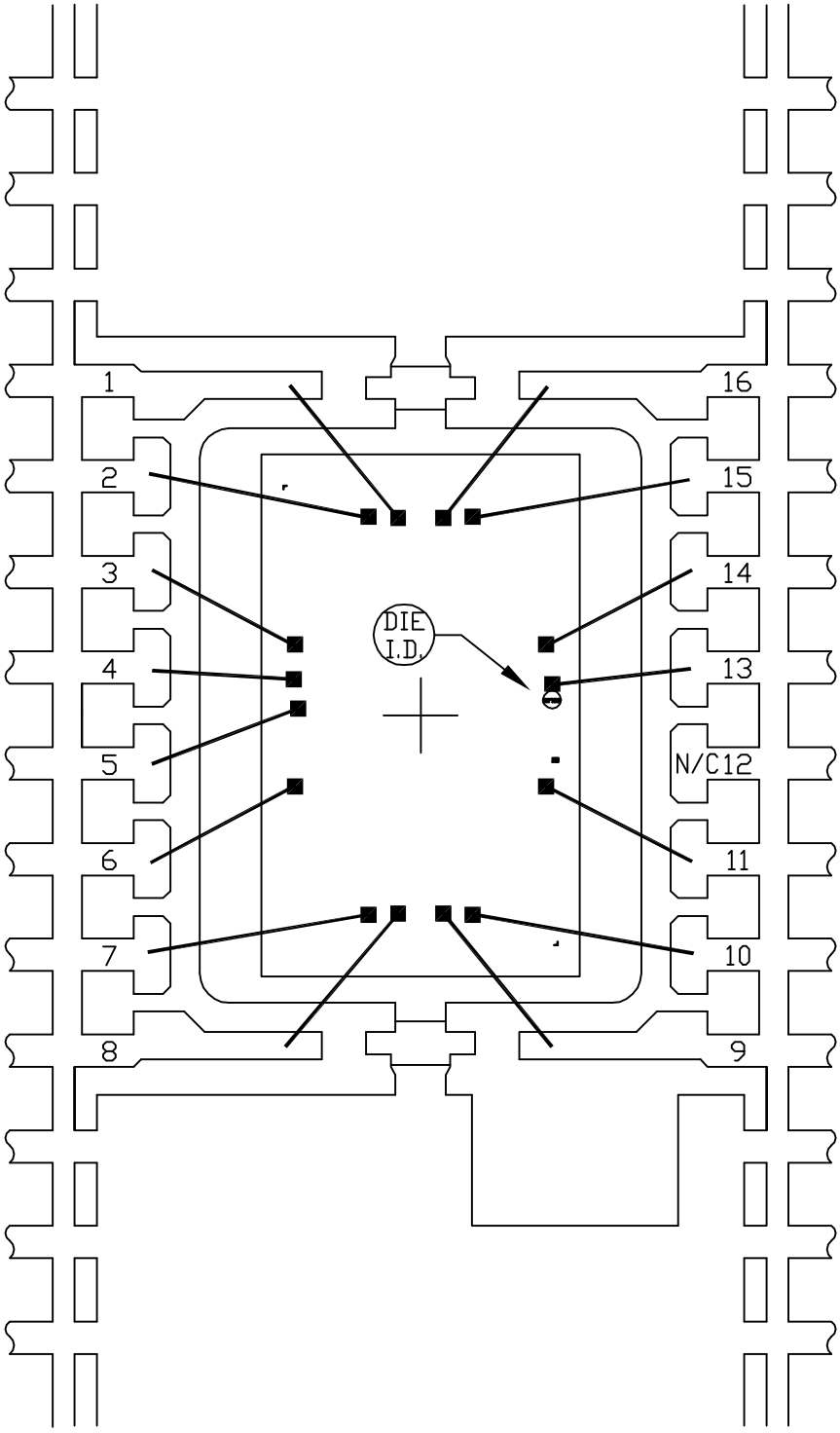
Mil Std 883D
Method 3015.7
Notice 8



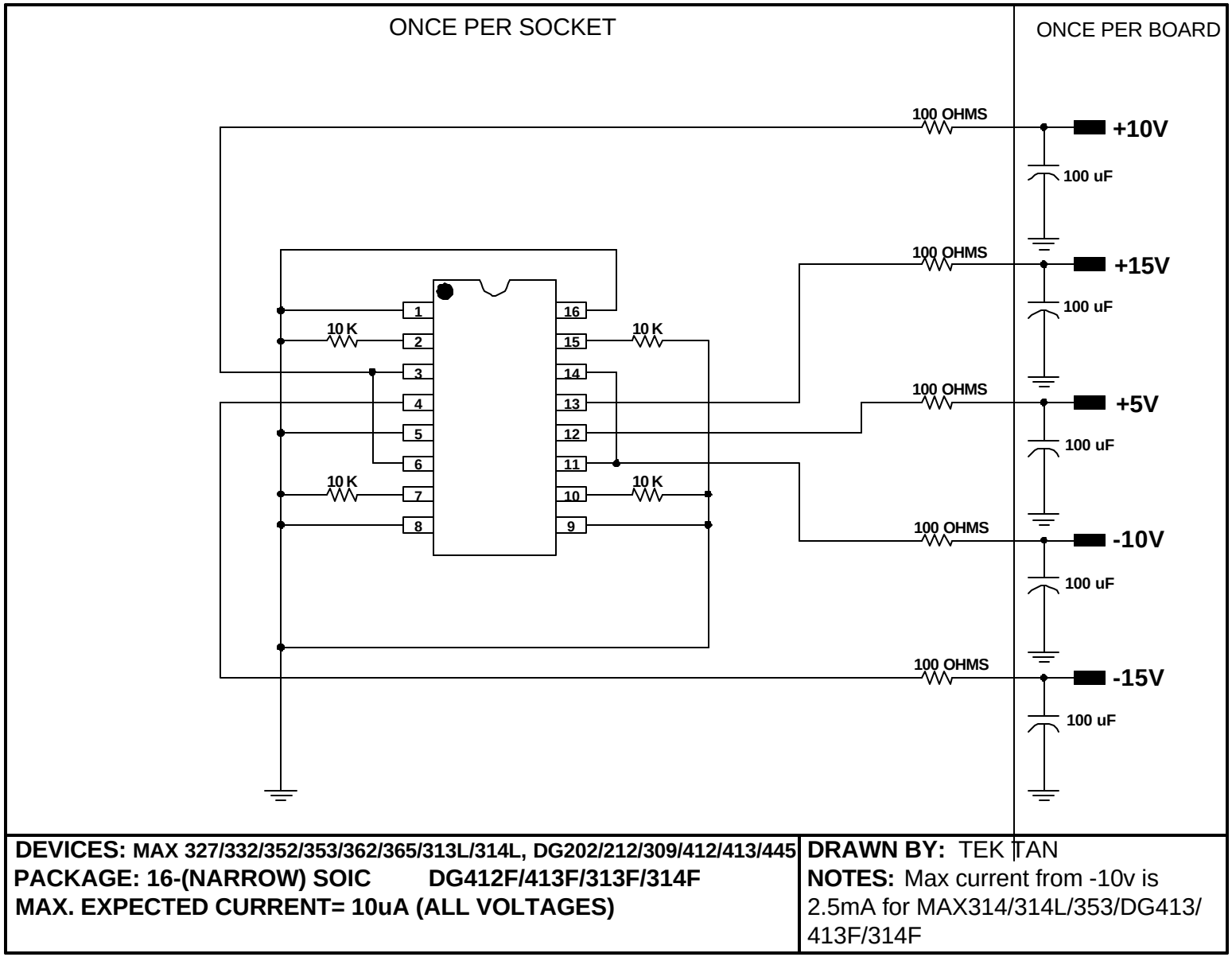
PKG. CODE: S16-8		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 102X220	PKG.			BOND DIAGRAM #: 05-1201-0253	REV: A
	DESIGN				



PKG. CODE: P16-2		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 140x170	PKG.			BOND DIAGRAM #: 05-1201-0252	REV: A
	DESIGN				



PKG. CODE: U16-1		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 118X154	PKG.			BOND DIAGRAM #: 05-1201-0254	REV: A
	DESIGN				



DEVICES: **MAX 327/332/352/353/362/365/313L/314L, DG202/212/309/412/413/445**
PACKAGE: 16-(NARROW) SOIC DG412F/413F/313F/314F
MAX. EXPECTED CURRENT= 10uA (ALL VOLTAGES)

DRAWN BY: TEK TAN
NOTES: Max current from -10v is 2.5mA for MAX314/314L/353/DG413/413F/314F