

RELIABILITY REPORT
FOR
MAX303xxE
PLASTIC ENCAPSULATED DEVICES

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MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

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Conclusion

The MAX303 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX303 is a precision, dual, high-speed analog switch. The single-pole double-throw (SPDT) MAX303 has two normally open (NO) and two normally closed (NC) poles. This part offers low on resistance (less than 35Ω), guaranteed to match to within 2Ω between channels and to remain flat over the full analog signal range ($\Delta 3\Omega$ max). It also offers low leakage (less than 250pA at +25°C and less than 6nA at +85°C) and fast switching (turn-on time less than 150ns and turn-off time less than 100ns).

The MAX303 is fabricated with Maxim's new improved silicon-gate process for high system accuracy. Design improvements guarantee extremely low charge injection (15pC) and low power consumption (35μW). A 44V maximum breakdown voltage allows rail-to-rail analog signal capability.

This monolithic switch operates with a single positive supply (+10V to +30V) or with split supplies ($\pm 4.5V$ to $\pm 20V$) while retaining CMOS-logic input compatibility and fast switching. CMOS inputs provide reduced input loading.

B. Absolute Maximum Ratings

<u>Item</u>	<u>Rating</u>
Voltage Referenced to V-	
V+	44V
GND	25V
V _L	(GND - 0.3V) to (V+ +0.3V)
NO_, NC_, IN_, COM_	(V- - 2V) to (V+ + 2V) or 30mA
Continuous Current, COM_, NO_, NC_	30mA
Peak Current, COM_, NO_, NC_ (pulsed at 1ms, 10% duty cycle max)	100mA
Storage Temp.	-65°C to +150°C
Lead Temp. (10 sec.)	+300°C
Power Dissipation	696mW
Derates above +70°C	8.70mW/°C
Continuous Power Dissipation (TA = +70°C)	
16-Pin PDIP	842mW
16-Pin SO	696mW
Derates above +70°C	
16-Pin PDIP	10.53mW/°C
16-Pin SO	8.70mW/°C

Note 1: Signals on NC_, NO_, or COM_ beyond V+ or V- are clamped by internal diodes. Limit forward diode current to maximum current rating.

II. Manufacturing Information

A. Description/Function:	Precision, Dual, High-Speed Analog Switch
B. Process:	S5 ((SG5) - Standard 5 micron silicon gate CMOS)
C. Number of Device Transistors:	66
D. Fabrication Location:	Oregon, USA
E. Assembly Location:	Philippines, Malaysia or Thailand
F. Date of Initial Production:	August, 1994

III. Packaging Information

A. Package Type:	16-Lead NSO	16-Lead PDIP
B. Lead Frame:	Copper	Copper
C. Lead Finish:	Solder Plate	Solder Plate
D. Die Attach:	Silver-filled Epoxy	Silver-filled Epoxy
E. Bondwire:	Gold (1.3 mil dia.)	Gold (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	# 05-0301-0539	# 05-0301-0538
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1	Level 1

IV. Die Information

A. Dimensions:	70 x 102 mils
B. Passivation:	Si ₃ N ₄ /SiO ₂ (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	5 microns (as drawn)
F. Minimum Metal Spacing:	5 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO ₂
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:

Jim Pedicord (Manager, Rel Operations)
Bryan Preeshl (Executive Director of QA)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4389 \times 300 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

└ Thermal acceleration factor assuming a 0.8eV activation energy

$$\lambda = 3.62 \times 10^{-9} \quad \lambda = 3.62 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure the reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on lots exceeding this level. The following Burn-In Schematic (Spec. # 06-1727) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1K**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The AG58-1 die type has been found to have all pins able to withstand a transient pulse of $\pm 800\text{V}$, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of $\pm 250\text{mA}$.

Table 1
Reliability Evaluation Test Results

MAX303xxE

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		240	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	NSO	77	0
			PDIP	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.

2/ No connects are not to be tested.

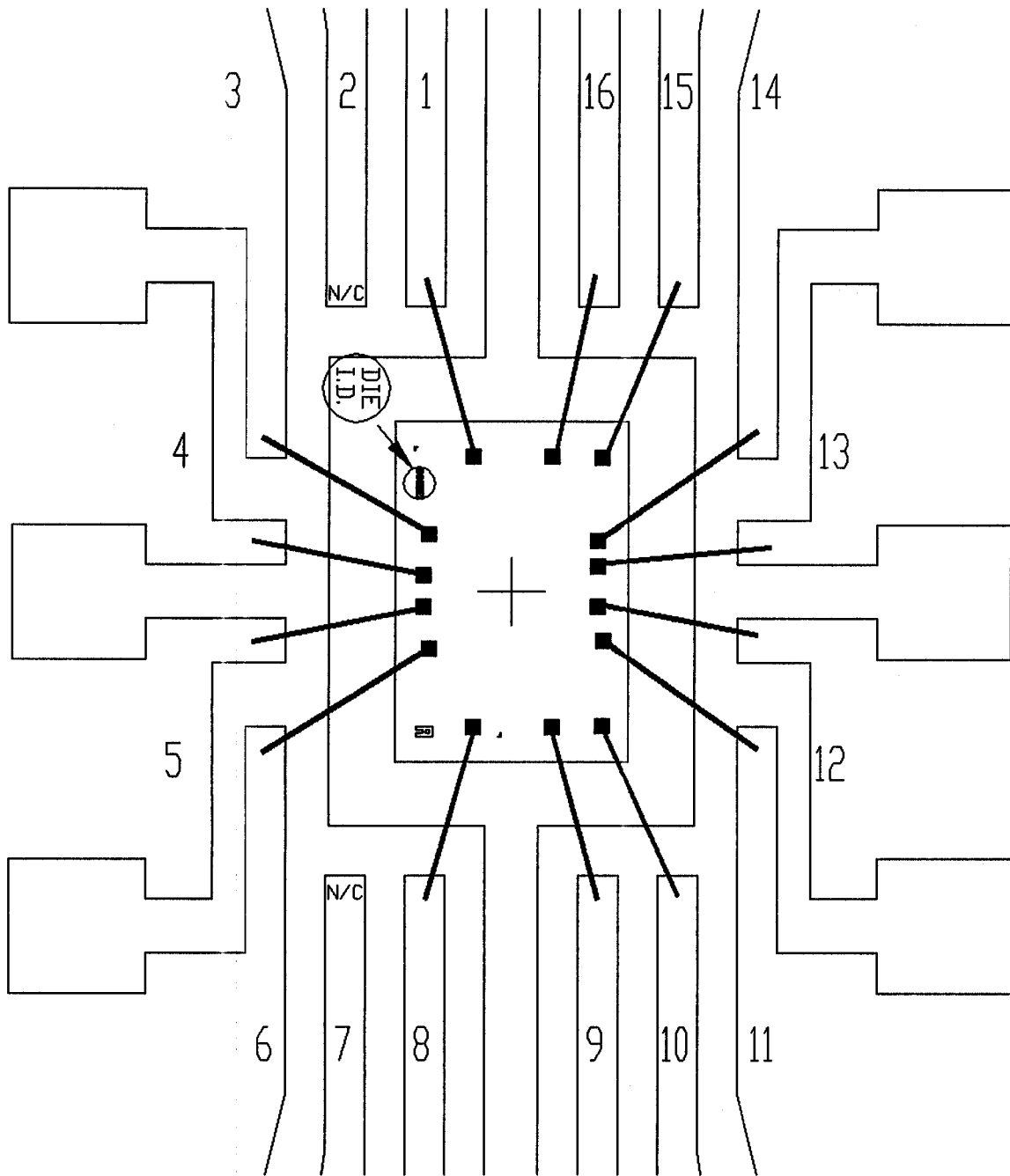
3/ Repeat pin combination 1 for each named Power supply and for ground

(e.g., where V_{PS1} is V_{DD} , V_{CC} , V_{SS} , V_{BB} , GND , $+V_S$, $-V_S$, V_{REF} , etc).

3.4 Pin combinations to be tested.

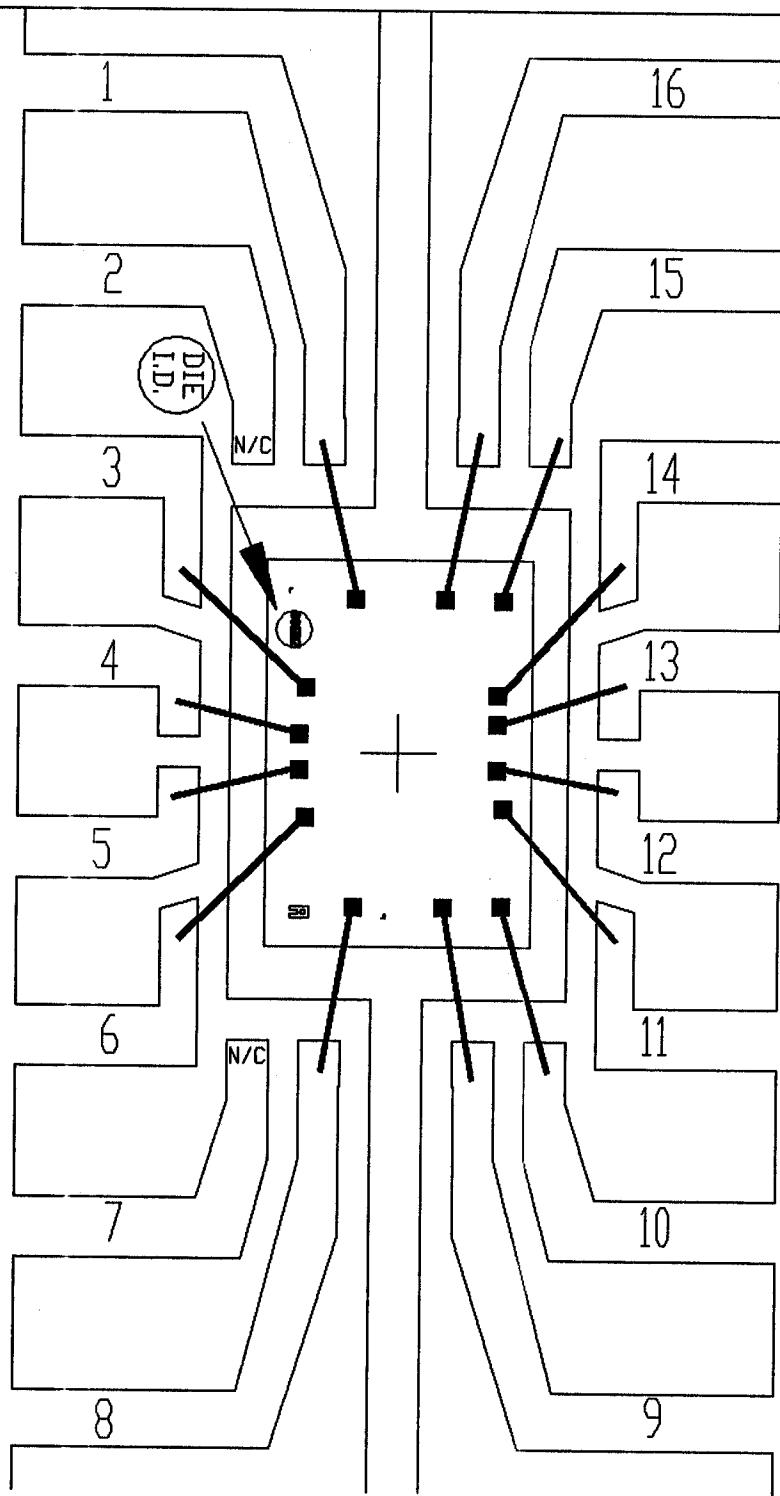
- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1} , or V_{SS2} or V_{SS3} or V_{CC1} , or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.





NOTE: DIE ORIENTATION
SHOWN IN CIRCLE

PKG.CODE: P16-1		APPROVALS	DATE	MAXIM	
CAV./PAD SIZE: 110 X 140	PKG. DESIGN			BUILDSHEET NUMBER: 05-0301-0538	REV.: B



NOTE: DIE ORIENTATION
SHOWN IN CIRCLE

PKG. CODE: S16-2	
CAV./PAD SIZE: 90 X 130	PKG. DESIGN

APPROVALS

DATE

MAXIM	
BUILDSHEET NUMBER: 05-0301-0539	REV.: B

