

RELIABILITY REPORT
FOR
MAX3023Exx
PLASTIC ENCAPSULATED DEVICES

July 17, 2006

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.
SUNNYVALE, CA 94086

Written by

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Conclusion

The MAX3023 has completed qualification testing except for product level Burn-In. Package and Process qualification has been completed for the device.

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I. Device Description

A. General

The MAX3023 single-/dual-/quadlevel translator provides the level shifting necessary to allow 100Mbps data transfer in a multivoltage system. Externally applied voltages, V_{CC} and V_L , set the logic levels on either side of the device. Logic signals present on the V_L side of the device appear as a higher voltage logic signal on the V_{CC} side of the device, and viceversa.

The MAX3023 (UCSP™ package) quad-level translator features an enable (EN) input. The MAX3023 (TSSOP package) quad-level translator features EN and EN inputs. When disabled, each device places all inputs/outputs on both sides in tri-state and reduces the V_{CC} supply current to 0.03 μ A, and the V_L supply current to 0.1 μ A. This device operate at a guaranteed 100Mbps data rate for $V_L > 1.8V$.

The MAX3023 accepts a +1.65V to +3.6V V_{CC} voltage and a +1.2V to ($V_{CC} - 0.4V$) V_L voltage, making it ideal for data transfer between low-voltage ASICs/programmable logic devices (PLDs) and higher voltage systems. The MAX3023 is available in 4 x 3 UCSP and 14-pin TSSOP packages. This device operates over the extended -40°C to +85°C temperature range.

B. Absolute Maximum Ratings

<u>Item</u>	<u>Rating</u>
All voltages are referenced to GND.	
V_{CC}	-0.3V to +4V
V_L	-0.3V to +4V
I/O $V_{CC_}$	-0.3V to ($V_{CC} + 0.3V$)
I/O $V_L_$	-0.3V to ($V_L + 0.3V$)
EN, EN	-0.3V to ($V_L + 0.3V$)
Short-Circuit Duration I/O $V_L_$, I/O $V_{CC_}$ to GND	Continuous
Continuous Power Dissipation ($T_A = +70^\circ C$)	
12-Bump UCSP (derate 6.5mW/°C above +70°C)	518.8mW
14-Pin TSSOP (derate 9.1mW/°C above +70°C)	727mW
Operating Temperature Range	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

II. Manufacturing Information

A. Description/Function:	+1.2V to +3.6V, 0.1 μ A, 100Mbps, Single-/Dual-/Quad-Level Translators
B. Process:	S4
C. Number of Device Transistors:	791
D. Fabrication Location:	California, USA
E. Assembly Location:	Philippines, Malaysia, Thailand, or USA
F. Date of Initial Production:	April, 2004

III. Packaging Information

A. Package Type:	14-Pin TSSOP	4 x 3 UCSP-12
B. Lead Frame:	Copper	N/A
C. Lead Finish:	Solder Plate or 100% Matte Tin	N/A
D. Die Attach:	Silver-Filled Epoxy	N/A
E. Bondwire:	Gold (1.3 mil dia.)	N/A
F. Mold Material:	Epoxy with silica filler	N/A
G. Assembly Diagram:	#05-9000-1051	#05-9000-1052
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C:	Level 1	Level 1

IV. Die Information

A. Dimensions:	80 x 61 mils
B. Passivation:	Si ₃ N ₄ /SiO ₂ (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1, Metal2 & Metal3 = 0.6 microns (as drawn)
F. Minimum Metal Spacing:	Metal1, Metal2 & Metal3 = 0.4 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO ₂
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

- A. Quality Assurance Contacts: Jim Pedicord (Manager, Rel Operations)
Bryan Preeshl (Managing Director of QA)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are pending. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 45 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

△ Temperature Acceleration factor assuming an activation energy of 0.8eV

$$\lambda = 24.43 \times 10^{-9}$$

$$\lambda = 24.43 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-6234) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1N**). Current monitor data for the S4 Process results in a FIT Rate of 0.37 @ 25C and 6.28 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The RT63 die type has been found to have all pins able to withstand a transient pulse of $\pm 2000\text{V}$ per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of $\pm 250\text{mA}$.

Table 1
Reliability Evaluation Test Results

MAX3023Exxxx

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		45	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	TSSOP	77	0
			UCSP	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	TSSOP UCSP	77 N/A	0 N/A
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality	TSSOP	77	0
			UCSP	77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic Package/Process data

Note 3: UCSP Temperature Cycle performed at -40°/125°C, 1000 Cycles, ramp rate 11°C/minute, dwell=15 minutes, One cycle/hour.

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.

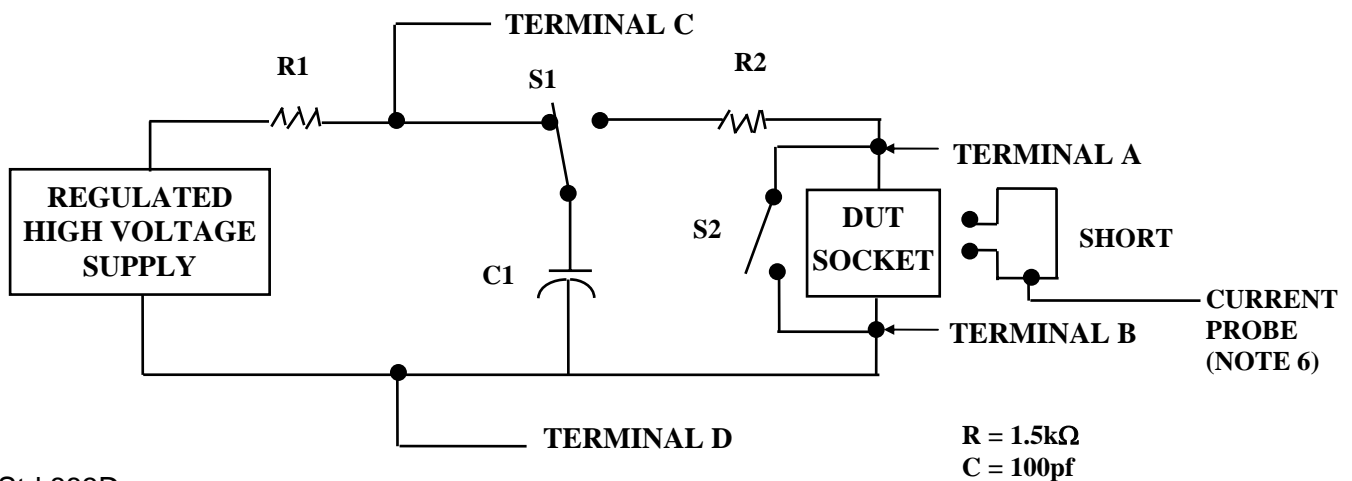
2/ No connects are not to be tested.

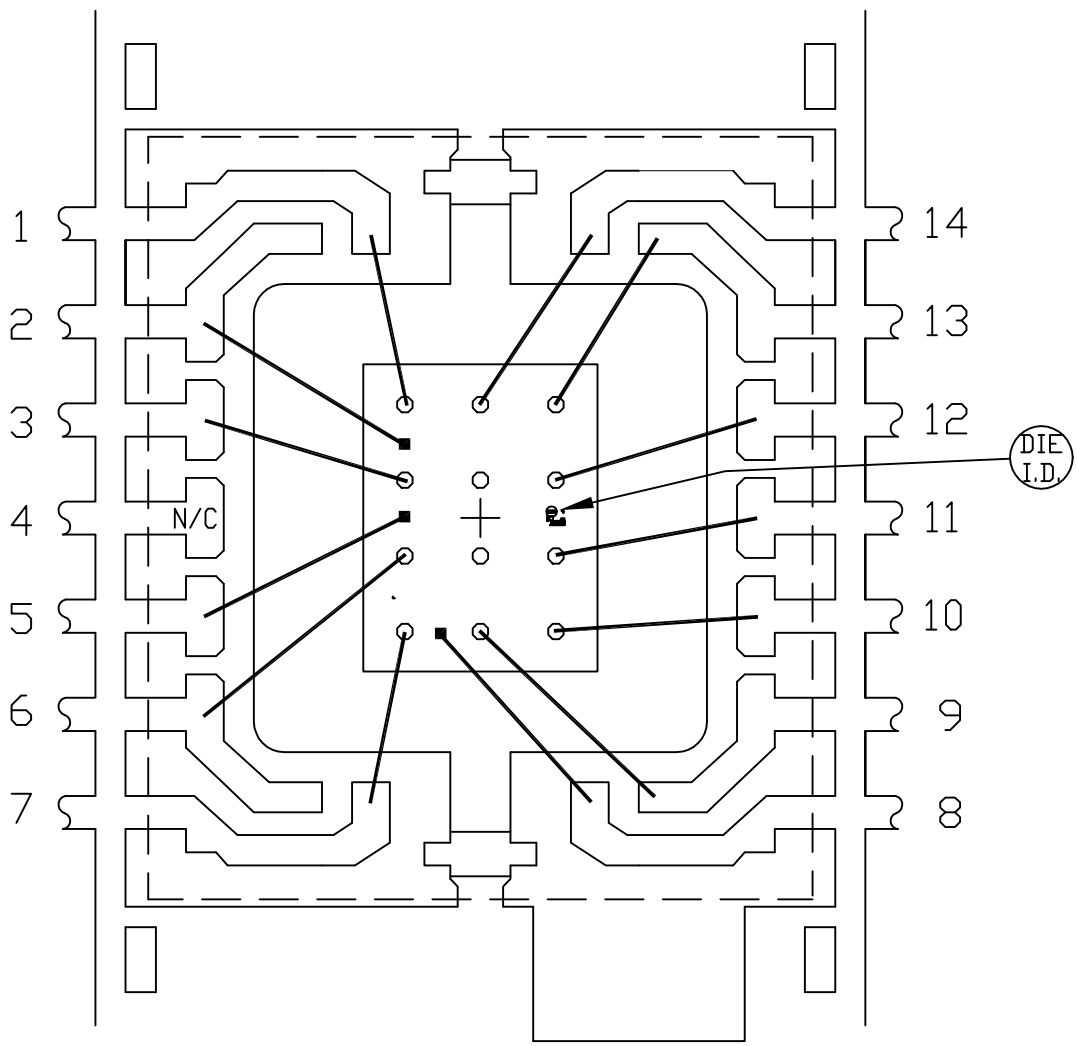
3/ Repeat pin combination I for each named Power supply and for ground

(e.g., where V_{PS1} is V_{DD} , V_{CC} , V_{SS} , V_{BB} , GND, $+V_S$, $-V_S$, V_{REF} , etc).

3.4 Pin combinations to be tested.

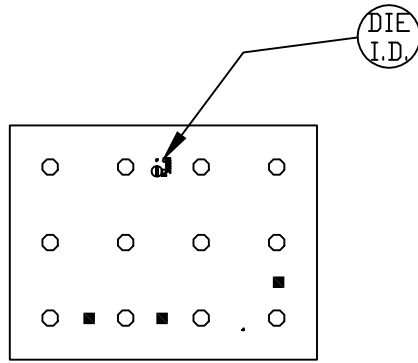
- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1} , or V_{SS2} or V_{SS3} or V_{CC1} , or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



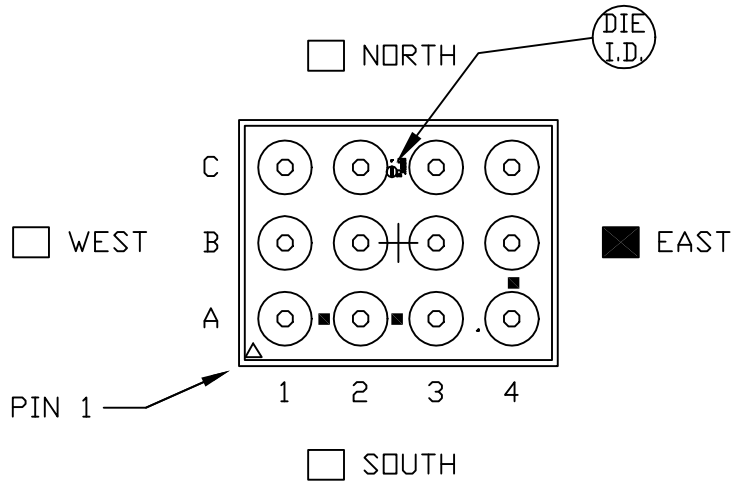


PKG. CODE: U14-1		SIGNATURES	DATE	 CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 118x122	PKG. DESIGN			BOND DIAGRAM #: 05-9000-1051	REV: A

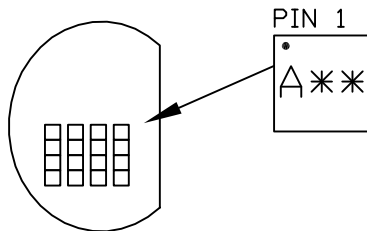
ORIGINAL CHIP



AFTER BUMP



SELECT THE BOX INDICATING THE WAFER FLAT SIDE WITH RESPECT TO PIN 1.



PART MARKING ORIENTATION IN REFERENCE TO WAFER FLAT (MARK IS ON WAFER BACKSIDE)

PKG. CODE: B12-1		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: N/A	PKG. DESIGN			BOND DIAGRAM #: 05-9000-1052	REV: A

