RELIABILITY REPORT

FOR

MAX3004ExP

PLASTIC ENCAPSULATED/CHIP SCALE DEVICES

August 11, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

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Conclusion

The MAX3004 sucessfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX3004 8-channel level translator provides the level shifting necessary to allow data transfer in a multivoltage system. Externally applied voltages, V_{CC} and V_L, set the logic levels on either side of the device. Logic signals present on the V_L side of the device appear as a higher voltage logic signal on the V_{CC} side of the device, and vice-versa.

The MAX3004 features an EN input that, when low, reduces the V_{CC} and V_L supply currents to <2µA. The MAX3002 operates at a guaranteed data rate of 20Mbps over the entire specified operating voltage range.

The MAX3004 accepts V_L voltages from +1.2V to +5.5V and V_{CC} voltages from +1.65V to +5.5V, making it ideal for data transfer between low-voltage ASICs/PLDs and higher voltage systems. The MAX3004 is available in 20-pin UCSP™ and 20-pin TSSOP packages.

B. Absolute Maximum Ratings

Item	Rating
All Voltages Referenced to GND	
VCC	-0.3V to +6V
VL	-0.3V to +6V
I/O VCC_	-0.3V to (VCC + 0.3V)
I/O VL_	-0.3V to (VL + 0.3V)
EN, EN A/B	-0.3V to +6V
Short-Circuit Duration I/O VL_, I/O VCC_ to GND	Continuous
Operating Temperature Ranges	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Continuous Power Dissipation (TA = +70°C)	
20-Pin TSSOP	559mW
20-Bump UCSP	800mW
Derates above +70°C	
20-Pin uMAX	7.0mW/°C
20-Bump UCSP	10.0mW/°C

II. Manufacturing Information

A. Description/Function:	+1.2V to +5.5V, 0.1µA, 35Mbps, 8-Channel Level Translators
B. Process:	S6
C. Number of Device Transistors:	1184
D. Fabrication Location:	California, USA
E. Assembly Location:	Philippines, Malaysia, Korea or USA
F. Date of Initial Production:	October, 2002

III. Packaging Information

	20-Lead TSSOP	**20-Bump UCSP**
A. Package Type:		
B. Lead Frame:	Copper	N/A
C. Lead Finish:	Solder Plate	N/A
D. Die Attach:	Silver-Filled Epoxy	N/A
E. Bondwire:	Gold (1.0 mil dia.)	N/A
F. Mold Material:	Epoxy with silica filler	N/A
G. Assembly Diagram:	# 05-2601-0092	# 05-2601-0093
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1	Level 1

IV. Die Information

A. Dimensions:	83 x 100 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Copper/Silicon
D. Backside Metallization:	None
E. Minimum Metal Width:	.6 microns (as drawn)
F. Minimum Metal Spacing:	.6 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:

Jim Pedicord	(Manager, Rel Operations)
Bryan Preeshl	(Executive Director of QA)
Kenneth Huening	(Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 45 \times 2}$$

(Chi square value for MTTF upper limit)

Thermal acceleration factor assuming a 0.8eV activation energy

$\lambda = 24.13 \times 10^{-9}$ $\lambda = 24.13$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure the reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on lots exceeding this level. The following Burn-In Schematic (Spec. #06-6004) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The RT50-2 die type has been found to have all pins able to withstand a transient pulse of 2000V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1
Reliability Evaluation Test Results

MAX3004ExP

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		45	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	TSSOP UCSP	77 77	0 0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	TSSOP UCSP	77 N/A	0 N/A
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010 (Note 3)	DC Parameters & functionality	TSSOP UCSP	77 77	0 0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data
Note 3: UCSP Temperature Cycle performed at -40°C/125°C, 1000 Cycles, ramp rate 11°C/minute, dwell=15 minutes, One cycle/hour

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

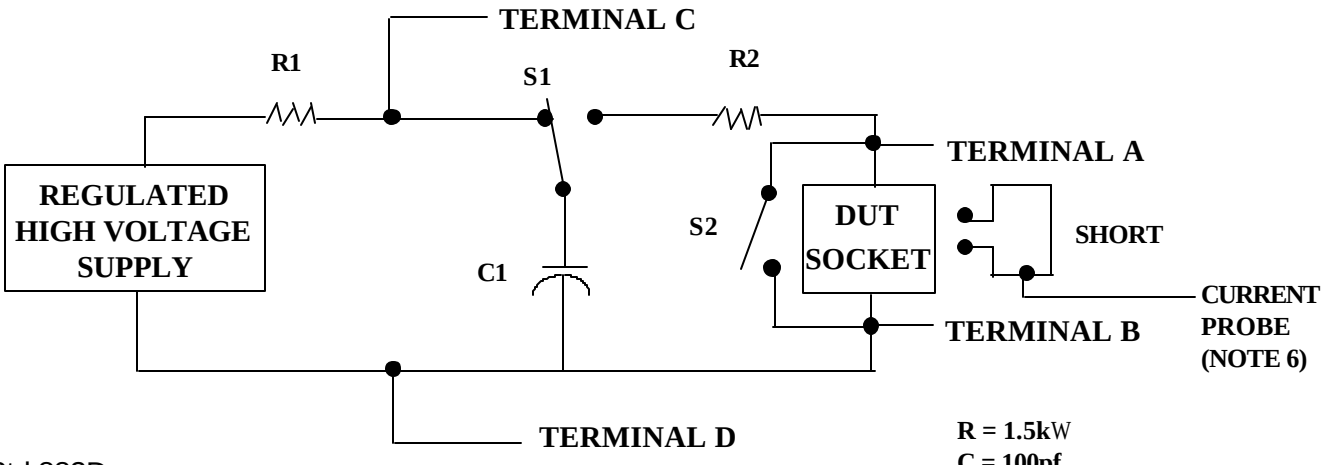
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

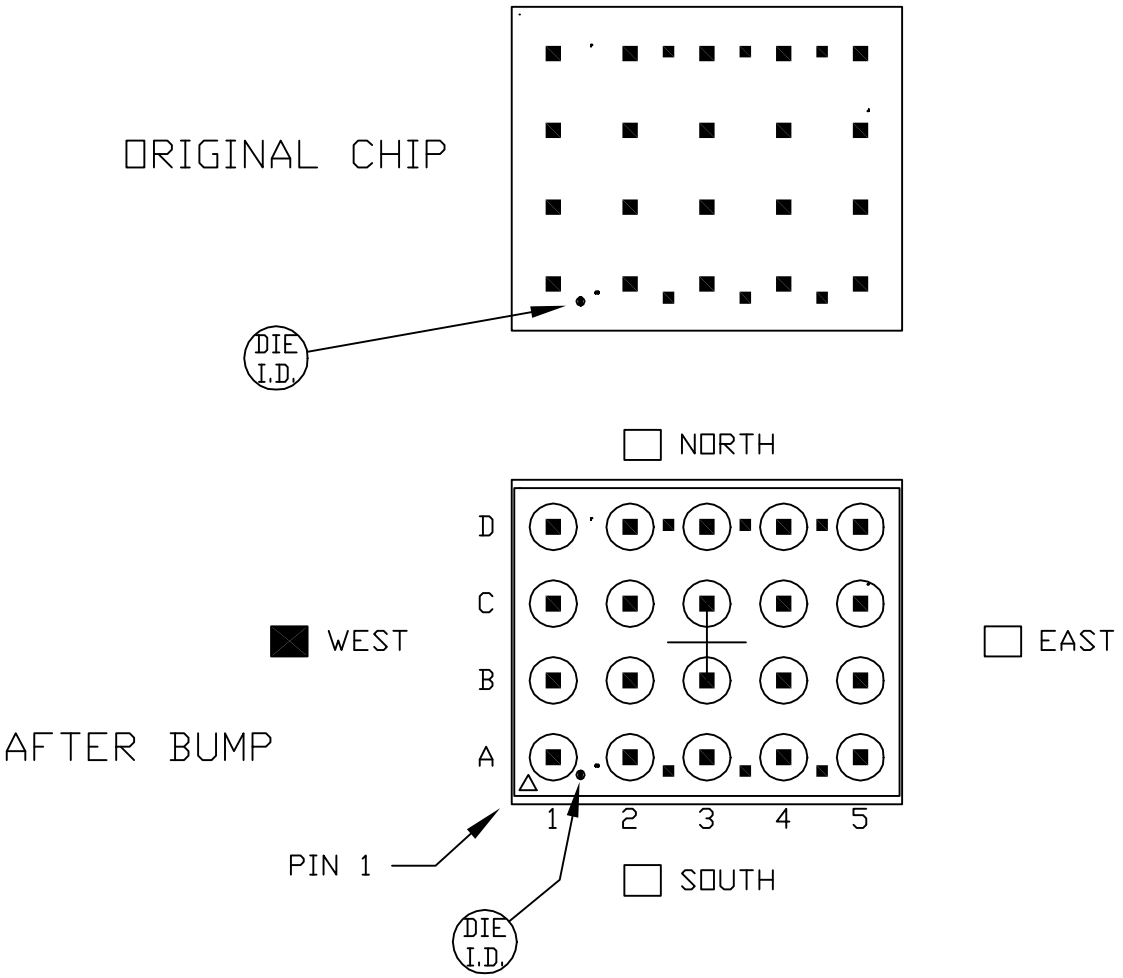
3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

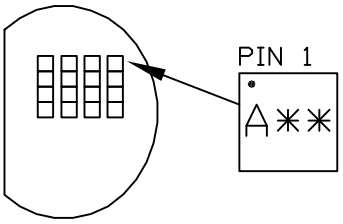
b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



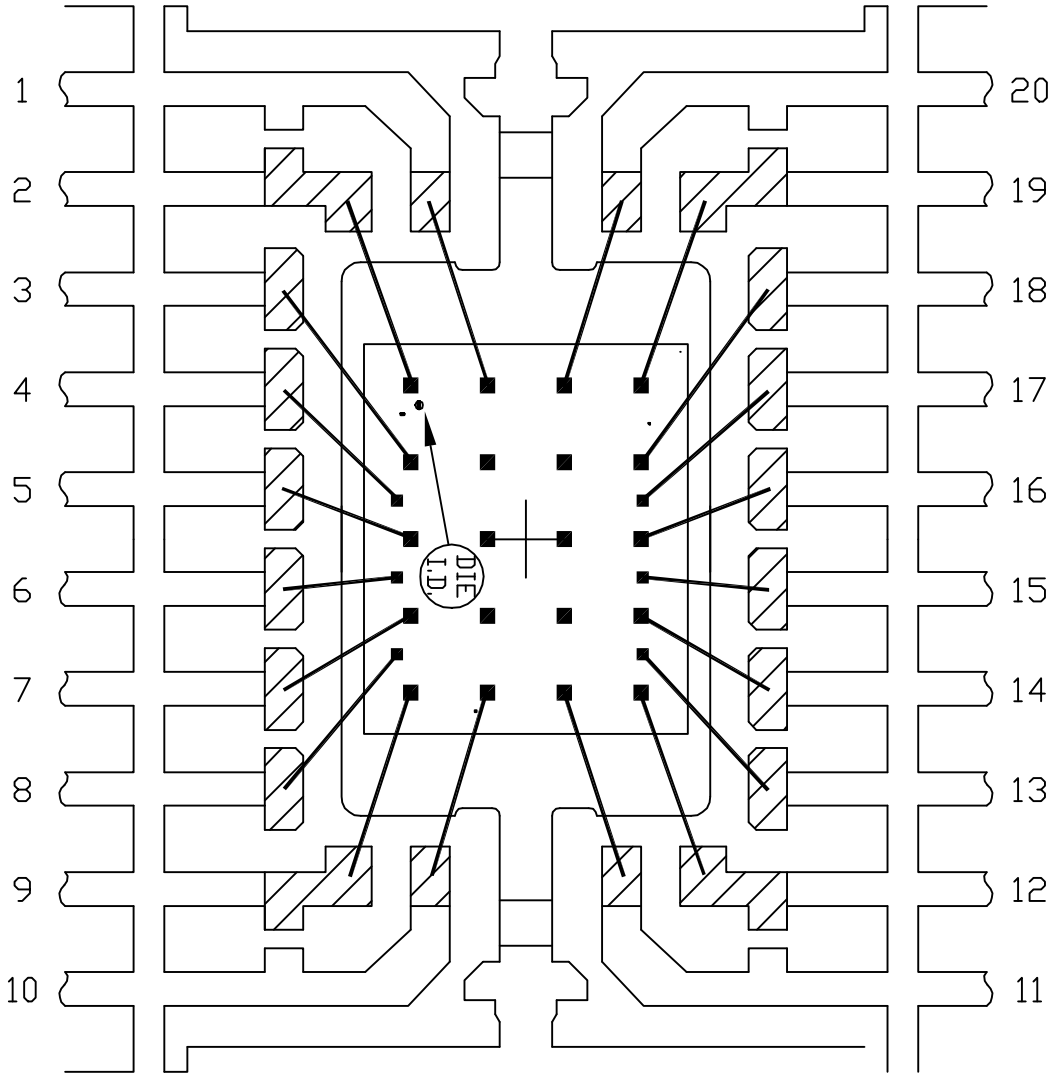


SELECT THE BOX INDICATING THE WAFER FLAT SIDE
WITH RESPECT TO PIN 1.



PART MARKING ORIENTATION
IN REFERENCE TO WAFER FLAT
(MARK IS ON WAFER BACKSIDE)

PKG. CODE: B20-1		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: N/A	PKG.			BOND DIAGRAM #: 05-2601-0093	REV: A
	DESIGN				

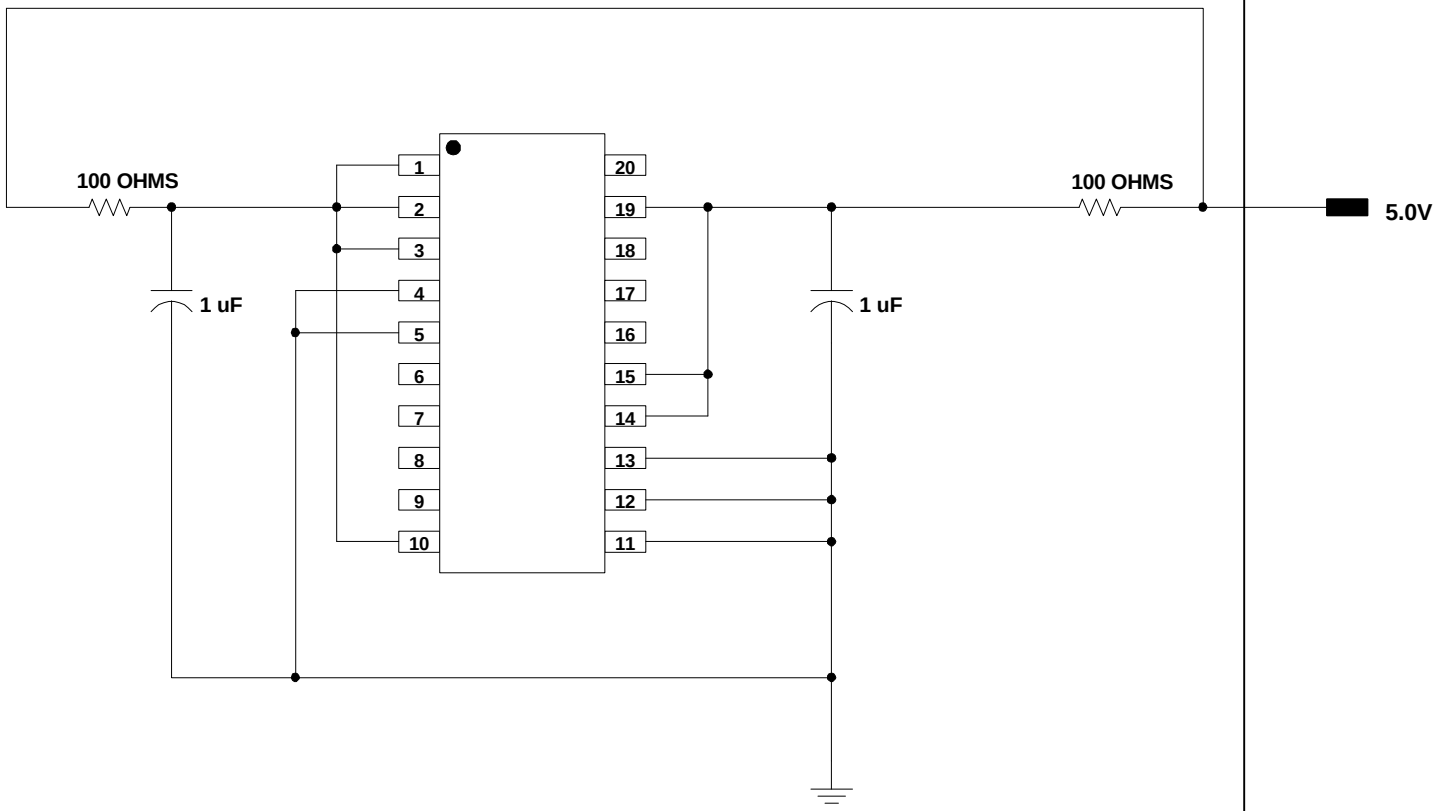


BONDABLE AREA

PKG. CODE: U20-3		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 95x142	PKG.			BOND DIAGRAM #: 05-2601-0092	REV: A
	DESIGN				

ONCE PER SOCKET

ONCE PER BOARD



DEVICES: MAX 3000 (RT50Z-P)
PACKAGE: 20-TSSOP
MAX. EXPECTED CURRENT = 1mA

DRAWN BY: TEK TAN
NOTES: