RELIABILITY REPORT

FOR

MAX3001EEUP+

PLASTIC ENCAPSULATED DEVICES

August 4, 2009

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Approved by
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Quality Assurance
Director, Reliability Engineering

Conclusion

The MAX3001EEUP+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim"s continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim"s quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX3000E/MAX3001E/MAX3002-MAX3012 8-channel level translators provide the level shifting necessary to allow data transfer in a multivoltage system. Externally applied voltages, VCC and VL, set the logic levels on either side of the device. Logic signals present on the VL side of the device appear as a higher voltage logic signal on the VCCside of the device, and vice-versa. The MAX3000E/MAX3001E/MAX3002/MAX3003 use an architecture specifically designed to be bidirectional without the use of a directional pin. The MAX3000E/MAX3001E/MAX3002/MAX3004-MAX3012 feature an EN input that, when low, reduces the VCC and VLsupply currents to CC side for greater protection in applications that route signals externally. The MAX3000E operates at a guaranteed datarate of 230kbps. The MAX3001E operates at a guaranteed data rate of 4Mbps. The MAX3002-MAX3012 operate at a guaranteed data rate of 20Mbps over the entire specified operating voltage range. The MAX3000E/MAX3001E/MAX3002-MAX3012 accept VL voltages from +1.2V to +5.5V and VCC voltages from +1.65V to +5.5V, making them ideal for data transfer between low-voltage ASICs/PLDs and higher voltage systems. The MAX3000E/MAX3001E/MAX3002-MAX3012 are available in 20-bump UCSP(tm), 20-pin TQFN (5mm x 5mm), and 20-pin TSSOP packages.

II. Manufacturing Information

A. Description/Function:	+1.2V to +5.5V, ±15kV ESD-Protected, 0.1µA, 35Mbps, 8-Channel Level Translators
B. Process:	C6
C. Number of Device Transistors:	
D. Fabrication Location:	California
E. Assembly Location:	Philippines, Malaysia
F. Date of Initial Production:	October 26, 2002

III. Packaging Information

A. Package Type:	20-pin TSSOP
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive Epoxy
E. Bondwire:	Gold (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-2601-0092
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	91°C/W
K. Single Layer Theta Jc:	20°C/W
L. Multi Layer Theta Ja:	73.8°C/W
M. Multi Layer Theta Jc:	20°C/W

IV. Die Information

A. Dimensions:	100 X 83 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.6 microns (as drawn)
F. Minimum Metal Spacing:	0.6 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Ken Wendel (Director, Reliability Engineering) Bryan Preeshl (Managing Director of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 138 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 7.8 \times 10^{-9}$

$\lambda = 7.8$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly 1000 hour life test monitors on its processes. This data is published in the Product Reliability Report found at http://www.maxim-ic.com/. Current monitor data for the C6 Process results in a FIT Rate of 1.6 @ 25C and 19.9 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

The industry standard 85°C/85%RH or HAST testing is monitored per device process once a quarter.

C. E.S.D. and Latch-Up Testing

The RT50-1 die type has been found to have all pins able to withstand a HBM transient pulse of:

HBM ESD: +/-2500 V per JEDEC JESD22-A114
CDM ESD: +/-750 V per JEDEC JESD22-C101

Latch-Up testing has shown that this device withstands a current of +/-250 mA.

Table 1
Reliability Evaluation Test Results

MAX3001EEUP+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	138	0
Moisture Testing (Note 2)				
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data