



RELIABILITY REPORT
FOR
MAX280EWE+T
PLASTIC ENCAPSULATED DEVICES

May 8, 2017

MAXIM INTEGRATED

160 RIO ROBLES
SAN JOSE, CA 95134

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Conclusion

The MAX280EWE+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX280/MXL1062 are 5th-order all-pole instrumentation lowpass filters with no DC error. The filter uses an external resistor and capacitor to isolate the integrated circuit from the DC signal path, thus providing excellent DC accuracy. The resistor and capacitor, along with the on-chip 4th-order switched capacitor filter, form a 5th-order low pass filter. Two MAX280/MXL1062s can be cascaded to form a 10th-order lowpass filter. The filter cutoff frequency is set by an internal clock which can be externally driven. The clock to cutoff-frequency ratio is 100:1, allowing clock ripple to be easily removed. The MAX280 is an enhanced version of the MXL1062. Enhancements include tighter specifications on the internal clock oscillator frequency and the buffer amplifier offset voltage.

II. Manufacturing Information

A. Description/Function:	5th-Order, Zero DC Error, Lowpass Filter
B. Process:	SG5
C. Fabrication Location:	USA
D. Assembly Location:	Philippines, Malaysia
E. Date of Initial Production:	Pre 1997

III. Packaging Information

A. Package Type:	16-pin SOIC (W)
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-0201-0048
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	105°C/W
K. Single Layer Theta Jc:	22°C/W
L. Multi Layer Theta Ja:	70°C/W
M. Multi Layer Theta Jc:	23°C/W

IV. Die Information

A. Dimensions:	94X115 mils
B. Passivation:	Si ₃ N ₄ /SiO ₂ (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Minimum Metal Width:	5.0 microns (as drawn)
E. Minimum Metal Spacing:	5.0 microns (as drawn)
F. Isolation Dielectric:	SiO ₂
G. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

- A. Quality Assurance Contacts: Eric Wright (Reliability Engineering)
Brian Standley (Manager, Reliability)
Bryan Preeshl (Vice President of QA)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% for all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 977 \times 4340 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 1.13 \times 10^{-9}$$

$$\lambda = 1.13 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at <http://www.maximintegrated.com/qa/reliability/monitor>. Cumulative monitor data for the SG5 Process results in a FIT Rate of 0.12 @ 25C and 2.04 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing

The AF04-2 die type has been found to have all pins able to withstand an HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-100mA and overvoltage per JEDEC JESD78.

Table 1
Reliability Evaluation Test Results

MAX280EWE+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135C Biased Time = 192 hrs.	DC Parameters & functionality	977	0	

Note 1: Life Test Data may represent plastic DIP qualification lots.