



RELIABILITY REPORT
FOR
MAX20313EWC+T
WAFER LEVEL DEVICES

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MAXIM INTEGRATED

160 RIO ROBLES
SAN JOSE, CA 95134

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Conclusion

The MAX20313EWC+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX20313–MAX20316 programmable current-limit switches feature internal current-limiting to prevent damage to host devices due to faulty load conditions. These current-limit switches feature a low, 10mΩ (typ) on-resistance and operate from a +2.5V to +5.5V input voltage range. The current limit is adjustable from 500mA to 6A, making these devices ideal for charging a large load capacitor and for high-current load-switching applications. The MAX20313 and MAX20315 feature a continuous current-limit mode during an overcurrent event. The MAX20314 and MAX20316 feature a latchoff mode during an overcurrent event. Additional safety features include thermal shutdown protection to prevent overheating and reverse current blocking to prevent current from being driven back into the source. The devices are available in a 12-bump (0.4mm pitch, 1.68mm x 1.48mm) wafer-level package (WLP) and operate over the -40°C to +85°C extended temperature range.

II. Manufacturing Information

A. Description/Function:	500mA to 6A Adjustable Current-Limit Switches
B. Process:	S18
C. Number of Device Transistors:	32057
D. Fabrication Location:	USA
E. Assembly Location:	Taiwan
F. Date of Initial Production:	July 7, 2017

III. Packaging Information

A. Package Type:	12-bump WLP
B. Lead Frame:	N/A
C. Lead Finish:	N/A
D. Bondwire:	N/A (N/A mil dia.)
E. Assembly Diagram:	#05-100406
F. Flammability Rating:	Class UL94-V0
G. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level
H. Single Layer Theta Ja:	N/A°C/W
I. Single Layer Theta Jc:	N/A°C/W
J. Multi Layer Theta Ja:	72.82°C/W
K. Multi Layer Theta Jc:	N/A°C/W

IV. Die Information

A. Dimensions:	67.3228X59.4488 mils
B. Passivation:	Si ₃ N ₄ /SiO ₂ (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Minimum Metal Width:	0.23 microns (as drawn)
E. Minimum Metal Spacing:	0.23 microns (as drawn)
F. Isolation Dielectric:	SiO ₂
G. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Eric Wright (Reliability Engineering) Brian Standley (Manager, Reliability) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% for all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 80 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 13.7 \times 10^{-9}$$

$$\lambda = 13.7 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at <http://www.maximintegrated.com/qa/reliability/monitor>. Cumulative monitor data for the S18 Process results in a FIT Rate of 0.40 @ 25C and 6.96 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing

The AO04-0 die type has been found to have all pins able to withstand an HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-100mA and overvoltage per JEDEC JESD78.

Table 1
Reliability Evaluation Test Results
MAX20313EWC+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135C	DC Parameters & functionality	80	0	
	Biased Time = 192 hrs.				

Note 1: Life Test Data may represent plastic DIP qualification lots.