

RELIABILITY REPORT  
FOR  
MAX19707ETM+  
PLASTIC ENCAPSULATED DEVICES

May 25, 2011

**MAXIM INTEGRATED PRODUCTS**

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## Conclusion

The MAX19707ETM+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

## Table of Contents

I. ....Device Description	IV. ....Die Information
II. ....Manufacturing Information	V. ....Quality Assurance Information
III. ....Packaging Information	VI. ....Reliability Evaluation
.....Attachments	

### I. Device Description

#### A. General

The MAX19707 is an ultra-low-power, mixed-signal analog front-end (AFE) designed for power-sensitive communication equipment. Optimized for high dynamic performance at ultra-low power, the device integrates a dual, 10-bit, 45Msps receive (Rx) ADC; dual, 10-bit, 45Msps transmit (Tx) DAC; three fast-settling 12-bit aux-DAC channels for ancillary RF front-end control; and a 10-bit, 333ksps housekeeping aux-ADC. The typical operating power in Tx-Rx FAST mode is 84.6mW at a 45MHz clock frequency. The Rx ADCs feature 54.2dB SNR and 71.2dBc SFDR at  $f_{IN} = 5.5\text{MHz}$  and  $f_{CLK} = 45\text{MHz}$ . The analog I/Q input amplifiers are fully differential and accept 1.024VP-P full-scale signals. Typical I/Q channel matching is  $\pm 0.03^\circ$  phase and  $\pm 0.01\text{dB}$  gain. The Tx DACs feature 73.2dBc SFDR at  $f_{OUT} = 2.2\text{MHz}$  and  $f_{CLK} = 45\text{MHz}$ . The analog I/Q full-scale output voltage is  $\pm 400\text{mV}$  differential. The Tx DAC common-mode DC level is programmable from 0.71V to 1.05V. The I/Q channel offset is programmable to optimize radio lineup sideband/carrier suppression. The typical I/Q channel matching is  $\pm 0.01\text{dB}$  gain and  $\pm 0.07^\circ$  phase. The Rx ADC and Tx DAC share a single, 10-bit parallel, high-speed digital bus allowing half-duplex operation for time-division duplex (TDD) applications. A 3-wire serial interface controls power-management modes, the aux-DAC channels, and the aux-ADC channels. The MAX19707 operates on a single 2.7V to 3.3V analog supply and 1.8V to 3.3V digital I/O supply. The MAX19707 is specified for the extended ( $-40^\circ\text{C}$  to  $+85^\circ\text{C}$ ) temperature range and is available in a 48-pin, thin QFN package. The *Selector Guide* at the end of the data sheet lists other pin-compatible versions in this AFE family.

## II. Manufacturing Information

A. Description/Function:	10-Bit, 45Msps, Ultra-Low-Power Analog Front-End
B. Process:	TS35
C. Number of Device Transistors:	
D. Fabrication Location:	Taiwan
E. Assembly Location:	China, Thailand
F. Date of Initial Production:	October 22, 2005

## III. Packaging Information

A. Package Type:	48-pin TQFN 7x7
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-1714
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	36°C/W
K. Single Layer Theta Jc:	1°C/W
L. Multi Layer Theta Ja:	25°C/W
M. Multi Layer Theta Jc:	1°C/W

## IV. Die Information

A. Dimensions:	143 X 163 mils
B. Passivation:	Si <sub>3</sub> N <sub>4</sub> /SiO <sub>2</sub> (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.35µm
F. Minimum Metal Spacing:	0.35µm
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO <sub>2</sub>
I. Die Separation Method:	Wafer Saw

## V. Quality Assurance Information

- A. Quality Assurance Contacts: Richard Aburano (Manager, Reliability Engineering)  
Don Lipps (Manager, Reliability Engineering)  
Bryan Preeshl (Vice President of QA)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.  
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

## VI. Reliability Evaluation

### A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate ( $\lambda$ ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 48 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 22.9 \times 10^{-9}$$

$$\lambda = 22.9 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at <http://www.maxim-ic.com/qa/reliability/monitor>. Cumulative monitor data for the TS35 Process results in a FIT Rate of 0.11 @ 25C and 1.93 @ 55C (0.8 eV, 60% UCL)

### B. E.S.D. and Latch-Up Testing (lot QJBCBQ002B D/C 0527)

The CA21-2 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA.

**Table 1**  
Reliability Evaluation Test Results

**MAX19707ETM+**

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
<b>Static Life Test</b> (Note 1)	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	48	0	QJBDAQ001B, D/C 0503

Note 1: Life Test Data may represent plastic DIP qualification lots.