

RELIABILITY REPORT
FOR
MAX1932ETC
PLASTIC ENCAPSULATED DEVICES

September 13, 2006

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

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Conclusion

The MAX1932 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX1932 generates a low-noise, high-voltage output to bias avalanche photodiodes (APDs) in optical receivers. Very low output ripple and noise is achieved by a constant-frequency, pulse-width modulated (PWM) boost topology combined with a unique architecture that maintains regulation with an optional RC or LC post filter inside its feedback loop. A precision reference and error amplifier maintain 0.5% output voltage accuracy.

The MAX1932 protects expensive APDs against adverse operating conditions while providing optimal bias. Traditional boost converters measure switch current for protection, whereas the MAX1932 integrates accurate high-side current limiting to protect APDs under avalanche conditions. A current-limit flag allows easy calibration of the APD operating point by indicating the precise point of avalanche breakdown. The MAX1932 control scheme prevents output overshoot and undershoot to provide safe APD operation without data loss.

The output voltage can be accurately set with either external resistors, an internal 8-bit DAC, an external DAC, or other voltage source. Output span and offset are independently settable with external resistors. This optimizes the utilization of DAC resolution for applications that may require limited output voltage range, such as 4.5V to 15V, 4.5V to 45V, 20V to 60V, or 40V to 90V.

B. Absolute Maximum Ratings

| <u>Item</u> | <u>Rating</u> |
|---|----------------------|
| VIN to GND | -0.3V to +6V |
| DIN, SCLK, CS, FB to GND | -0.3V to +6V |
| COMP, DACOUT, GATE, CL to GND | -0.3V to (VIN +0.3V) |
| CS+, CS- to GND | -0.3V to +110V |
| Operating Temperature Range | -40°C to +85°C |
| Junction Temperature | +150°C |
| Storage Temperature Range | -65°C to +150°C |
| Lead Temperature (soldering 10s) | +300°C |
| Continuous Power Dissipation (TA = +70°C) | |
| 12-Pin QFN (4x4) | 1349mW |
| Derates above +70°C | |
| 12-Pin QFN (4x4) | 16.9mW/°C |

II. Manufacturing Information

| | |
|----------------------------------|---|
| A. Description/Function: | Digitally Controlled, 0.5% Accurate, Safest APD Bias Supply |
| B. Process: | S12 (Standard 1.2 micron silicon gate CMOS) |
| C. Number of Device Transistors: | 1592 |
| D. Fabrication Location: | Oregon, USA |
| E. Assembly Location: | Thailand or Hong Kong |
| F. Date of Initial Production: | July, 2002 |

III. Packaging Information

| | |
|---|--------------------------------|
| A. Package Type: | 20-Lead QFN (4x4) |
| B. Lead Frame: | Copper |
| C. Lead Finish: | Solder Plate or 100% Matte Tin |
| D. Die Attach: | Silver-filled Epoxy |
| E. Bondwire: | Gold (1.0 mil dia.) |
| F. Mold Material: | Epoxy with silica filler |
| G. Assembly Diagram: | # 05-3501-0036 |
| H. Flammability Rating: | Class UL94-V0 |
| I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C: | Level 1 |

IV. Die Information

| | |
|----------------------------|---|
| A. Dimensions: | 81 x 81 mils |
| B. Passivation: | $\text{Si}_3\text{N}_4/\text{SiO}_2$ (Silicon nitride/ Silicon dioxide) |
| C. Interconnect: | Aluminum/Copper/Si |
| D. Backside Metallization: | None |
| E. Minimum Metal Width: | 1.2 microns (as drawn) |
| F. Minimum Metal Spacing: | 1.2 microns (as drawn) |
| G. Bondpad Dimensions: | 5 mil. Sq. |
| H. Isolation Dielectric: | SiO_2 |
| I. Die Separation Method: | Wafer Saw |

V. Quality Assurance Information

A. Quality Assurance Contacts:

Jim Pedicord (Manager, Reliability Operations)
Bryan Preeshl (Managing Director of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 45 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

└─ Thermal acceleration factor assuming a 0.8eV activation energy

$$\lambda = 24.43 \times 10^{-9} \quad \lambda = 24.43 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure the reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on lots exceeding this level. The following Burn-In Schematic (Spec. # 06-5987) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1N**). Current monitor data for the B8/S8 Process results in a FIT rate of 0.17 @ 25°C and 2.92 @ 55°C (eV = 0.8, UCL = 60%).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The PM14 die type has been found to have all pins able to withstand a transient pulse of $\pm 1500\text{V}$, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of $\pm 250\text{mA}$.

Table 1
Reliability Evaluation Test Results

MAX1932ETC

| TEST ITEM | TEST CONDITION | FAILURE IDENTIFICATION | PACKAGE | SAMPLE SIZE | NUMBER OF FAILURES |
|-----------------------------------|---|----------------------------------|---------|-------------|--------------------|
| Static Life Test (Note 1) | | | | | |
| | Ta = 150°C Biased Time = 192 hrs. | DC Parameters & functionality | | 45 | 0 |
| Moisture Testing (Note 2) | | | | | |
| Pressure Pot | Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs. | DC Parameters & functionality | QFN | 77 | 0 |
| 85/85 | Ta = 85°C RH = 85% Biased Time = 1000hrs. | DC Parameters & functionality | | 77 | 0 |
| Mechanical Stress (Note 2) | | | | | |
| Temperature Cycle | -65°C/150°C 1000 Cycles Method 1010 | DC Parameters & functionality | | 77 | 0 |

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic process/package data.

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

| | Terminal A (Each pin individually connected to terminal A with the other floating) | Terminal B (The common combination of all like-named pins connected to terminal B) |
|----|---|---|
| 1. | All pins except V_{PS1} 3/ | All V_{PS1} pins |
| 2. | All input and output pins | All other input-output pins |

1/ Table II is restated in narrative form in 3.4 below.

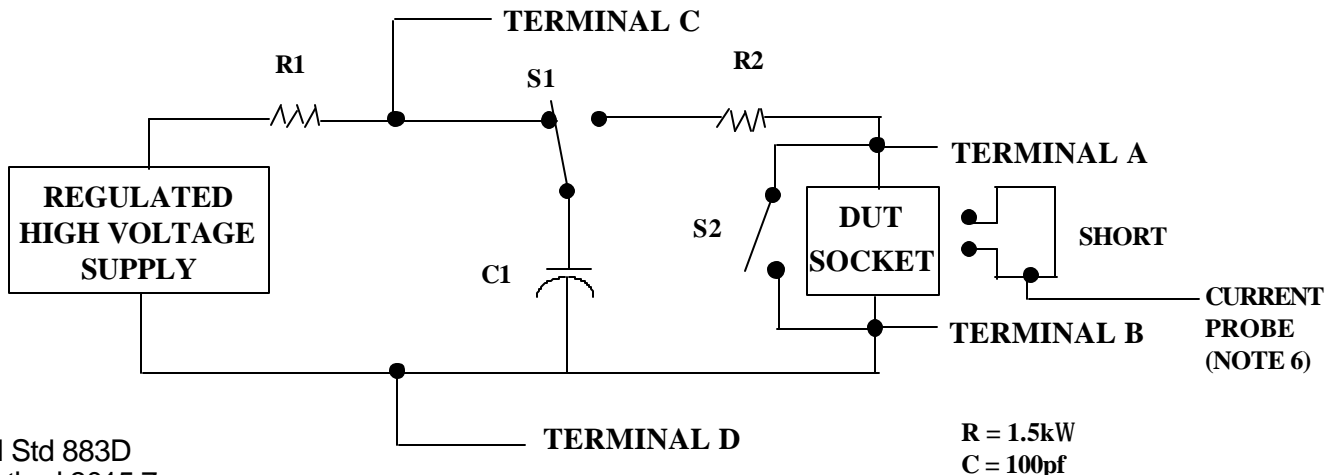
2/ No connects are not to be tested.

3/ Repeat pin combination I for each named Power supply and for ground

(e.g., where V_{PS1} is V_{DD} , V_{CC} , V_{SS} , V_{BB} , GND, $+V_S$, $-V_S$, V_{REF} , etc).

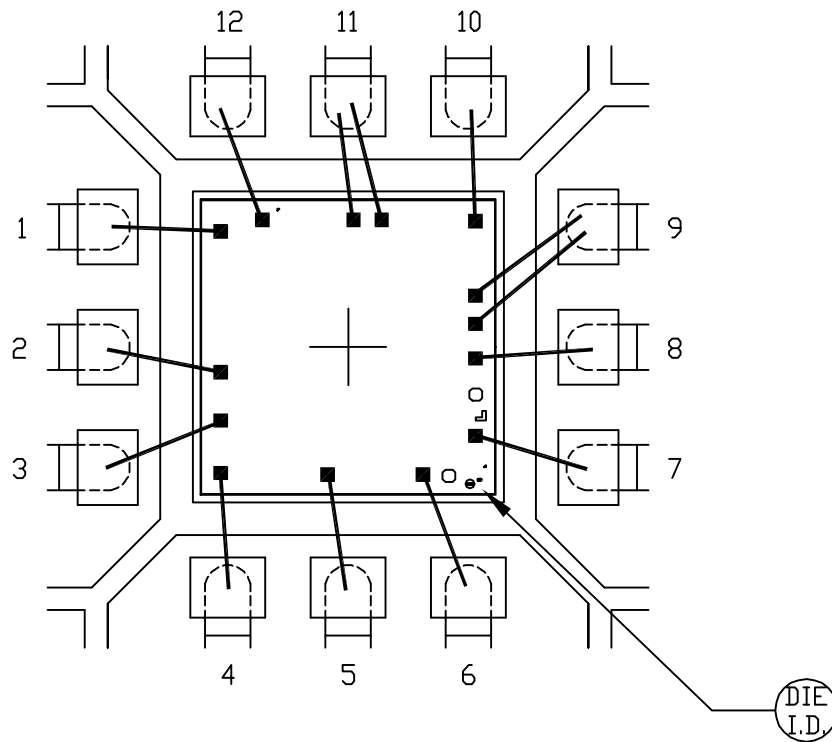
3.4 Pin combinations to be tested.

- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1} , or V_{SS2} or V_{SS3} or V_{CC1} , or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



4x4x0.8 MM QFN THIN PKG.

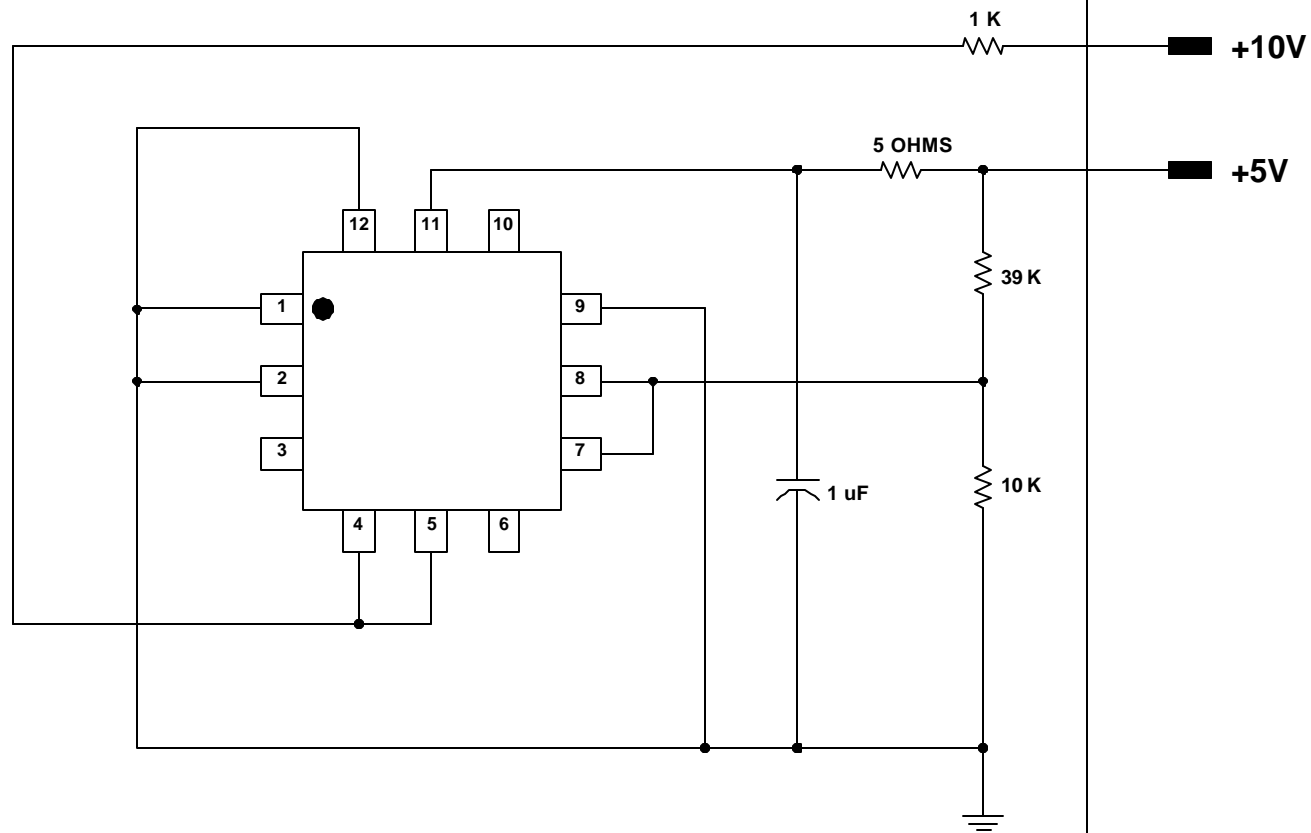
EXPOSED PAD PKG.



| | | | | | |
|-------------------------|----------------|----------------------------|--------------------|---|-----------|
| PKG. CODE: T1244-2 | | SIGNATURES | DATE |  CONFIDENTIAL & PROPRIETARY | |
| CAV./PAD SIZE: 98x98 | PKG. DESIGN | RAMON DE LEON ILLY KING | 6/20/02 6/20/02 | BOND DIAGRAM #: 05-3501-0036 | REV: B |

ONCE PER SOCKET

ONCE PER BOARD



DEVICES: MAX 1932
PACKAGE: 12-QFN (4x4).
MAX. EXPECTED CURRENT = 5mA (+5V), 5uA (10V).

DRAWN BY: TEK TAN
NOTES: