

RELIABILITY REPORT
FOR
MAX1886EZX+
PLASTIC ENCAPSULATED DEVICES

March 1, 2011

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.
SUNNYVALE, CA 94086

Approved by
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Conclusion

The MAX1886EZK+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX1886 is a high-current operational transconductance amplifier. The MAX1886 is ideal for driving the backplane of an active matrix, dot inversion thin film transistor (TFT) liquid crystal display (LCD). The MAX1886's high >500mA peak-current drive capability provides fast response to pulsed load conditions. The MAX1886 is stable from 0.47 μ F to an unlimited amount of output capacitance. The MAX1886 is available in the low-profile (1.1mm max) 5-pin Thin SOT23 package and fully specified over the -40°C to +85°C extended temperature range.

II. Manufacturing Information

A. Description/Function:	High-Current VCOM Drive Buffer
B. Process:	B8
C. Number of Device Transistors:	
D. Fabrication Location:	Oregon
E. Assembly Location:	Malaysia, Philippines
F. Date of Initial Production:	July 28, 2001

III. Packaging Information

A. Package Type:	5-pin TSOT
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-3801-0003
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	365.1°C/W
K. Single Layer Theta Jc:	75°C/W
L. Multi Layer Theta Ja:	N/A
M. Multi Layer Theta Jc:	N/A

IV. Die Information

A. Dimensions:	32 X 56 mils
B. Passivation:	Si ₃ N ₄ /SiO ₂ (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.8 microns (as drawn)
F. Minimum Metal Spacing:	0.8 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO ₂
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

- A. Quality Assurance Contacts: Richard Aburano (Manager, Reliability Engineering)
Don Lipps (Manager, Reliability Engineering)
Bryan Preeshl (Vice President of QA)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 76 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 31.9 \times 10^{-9}$$

$$\lambda = 31.9 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at <http://www.maxim-ic.com/qa/reliability/monitor>. Cumulative monitor data for the B8 Process results in a FIT Rate of 0.06 @ 25C and 0.99 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (ESD lot I4X0BQ001C D/C 0126, Latch-Up lot I4X0CQ001E D/C 0444)

The PD06 die type has been found to have all pins able to withstand a HBM transient pulse of +/-1000V per Mil-Std 883 Method 3015.7. Latch-Up testing has shown that this device withstands a current of +/-250mA.

Table 1
Reliability Evaluation Test Results

MAX1886EZK+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	76	1	I4X0BQ001E, D/C 0126

Note 1: Life Test Data may represent plastic DIP qualification lots.