

RELIABILITY REPORT
FOR
MAX1873xEEE
PLASTIC ENCAPSULATED DEVICES

February 10, 2004

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

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Conclusion

The MAX1873 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I.Device Description	V.Quality Assurance Information
II.Manufacturing Information	VI.Reliability Evaluation
III.Packaging Information	
IV.Die InformationAttachments

I. Device Description

The low-cost MAX1873 provides all functions needed to simply and efficiently charge 2-, 3-, or 4-series lithium-ion cells at up to 4A or more. It provides a regulated charging current and voltage with less than $\pm 0.75\%$ total voltage error at the battery terminals. An external P-channel MOSFET operates in a step-down DC-DC configuration to efficiently charge batteries in low-cost designs.

The MAX1873 regulates the battery voltage and charging current using two control loops that work together to transition smoothly between voltage and current regulation. An additional control loop limits current drawn from the input source so that AC adapter size and cost can be minimized. An analog voltage output proportional to charging current is also supplied so that an ADC or microcontroller can monitor charging current.

The MAX1873 may also be used as an efficient current-limited source to charge NiCd or NiMH batteries in multichemistry charger designs. The MAX1873 is available in a space-saving 16-pin QSOP package.

B. Absolute Maximum Ratings

<u>Item</u>	<u>Rating</u>
CSSP, CSSN, DCIN to GND	-0.3V to +30V
VL, ICHG/EN to GND	-0.3V to +6V
VH, EXT to DCIN	-6V to +0.3V
VH, EXT to GND	(VDCIN + 0.3V) to -0.3V
EXT to VH	+6V to -0.3V
DCIN to VL	+30V to -0.3V
VADJ, REF, CCI, CCV, CCS, IOUT to GND	-0.3V to (VL + 0.3V)
BATT, CSB to GND	-0.3V to +20V
CSSP to CSSN	-0.3V to +0.6V
CSB to BATT	-0.3V to +0.6V
VL Source Current	+50mA
VH Sink Current	+40mA
Operating Temperature Range	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Continuous Power Dissipation (TA = +70°C)	
16-Pin QSOP	667mW
Derates above +70°C	
16-Pin QSOP	8.3mW/°C

II. Manufacturing Information

A. Description/Function:	Simple Current-Limited Switch-Mode Li+ Charger Controller
B. Process:	S12 (Standard 1.2 micron silicon gate CMOS)
C. Number of Device Transistors:	1397
D. Fabrication Location:	Oregon, USA
E. Assembly Location:	Malaysia
F. Date of Initial Production:	July, 2001

III. Packaging Information

A. Package Type:	16-Lead QSOP
B. Lead Frame:	Copper
C. Lead Finish:	Solder Plate
D. Die Attach:	Silver-Filled Epoxy
E. Bondwire:	Gold (1.0 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	Buildsheet # 05-2301-0109
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1

IV. Die Information

A. Dimensions:	106 x 80 mils
B. Passivation:	$\text{Si}_3\text{N}_4/\text{SiO}_2$ (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Copper/Silicon
D. Backside Metallization:	None
E. Minimum Metal Width:	1.2 microns (as drawn)
F. Minimum Metal Spacing:	1.2 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:

Jim Pedicord (Manager, Reliability Operations)
Bryan Preeshl (Executive Director of QA)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4389 \times 46 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

└ Thermal acceleration factor assuming a 0.8eV activation energy

$$\lambda = 23.61 \times 10^{-9} \quad \lambda = 23.61 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure the reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on lots exceeding this level. The following Burn-In Schematic (Spec. #06-5755) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The PY96 die type has been found to have all pins able to withstand a transient pulse of +/-600V for MAX1873S, +/-800V for MAX1873R & MAX1873T, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of $\pm 250\text{mA}$.

Table 1
Reliability Evaluation Test Results

MAX1873xEEE

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	46	0
Moisture Testing (Note 2)				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots.

Note 2: Generic package/process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

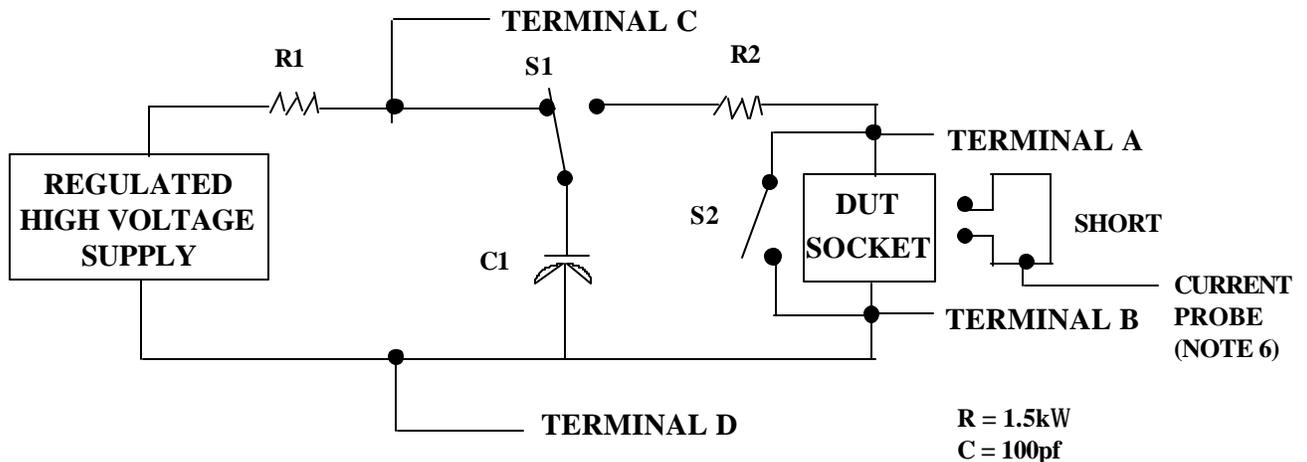
1/ Table II is restated in narrative form in 3.4 below.

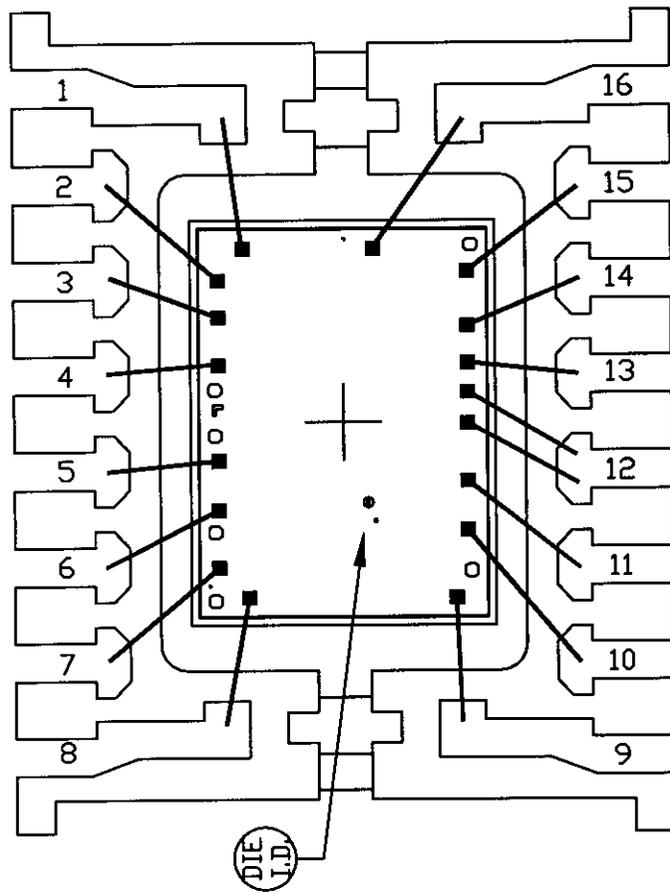
2/ No connects are not to be tested.

3/ Repeat pin combination I for each named Power supply and for ground (e.g., where V_{PS1} is V_{DD} , V_{CC} , V_{SS} , V_{BB} , GND, $+V_S$, $-V_S$, V_{REF} , etc).

3.4 Pin combinations to be tested.

- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1} , or V_{SS2} or V_{SS3} or V_{CC1} , or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.





PKG. CODE:
 E16-1

CAV./PAD SIZE:
 96X130

PKG.
 DESIGN

SIGNATURES

DATE

MAXIM
 CONFIDENTIAL & PROPRIETARY

BOND DIAGRAM #:
 05-2301-0109

REV:
 A

