MAX1858EEG
Rev. B

RELIABILITY REPORT

FOR

MAX1858EEG

PLASTIC ENCAPSULATED DEVICES

July 6, 2006

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

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Conclusion

The MAX1858 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX1858 dual, synchronized, step-down controller generates two outputs from input supplies ranging from 4.75V to 23V. Each output is adjustable from sub-1V to 18V and supports loads of 10A or higher. Input voltage ripple and total RMS input ripple current are reduced by synchronized 180° out-of-phase operation.

The switching frequency is adjustable from 100kHz to 600kHz with an external resistor. Alternatively, the controller can be synchronized to an external clock generated to another MAX1858 or a system clock. One MAX1858 can be set to generate an in-phase, or 90° out-of-phase, clock signal for synchronization with additional controllers. This allows two controllers to operate either as an interleaved two- or four-phase system with each output shifted by 90°. The device also features "first-on/last-off" power sequencing for compatibility with DSPs, ASICs, and FPGAs, as well as soft-start and soft-stop to ensure reliable and repeatable power sequencing.

The MAX1858 eliminates the need for current-sense resistors by utilizing the low-side MOSFET's on-resistance as a current-sense element. This protects the DC-DC components from damage during output-overload conditions or when output short-circuit faults without requiring a current-sense resistor. Adjustable foldback current limit reduces power dissipation during short-circuit condition. A power-on reset output signals the system when both outputs reach regulation.

B. Absolute Maximum Ratings

Item	Rating
V+ to GND	-0.3V to +25V
PGND to GND	-0.3V to +0.3V
VL to GND	-0.3V to the lower of +6V and (V+ + 0.3V)
BST1, BST2 to GND	-0.3V to +30V
LX1 to BST1	-6V to +0.3V
LX2 to BST2	-6V to +0.3V
DH1 to LX1	-0.3V to (VBST1 + 0.3V)
DH2 to LX2	-0.3V to (VBST2 + 0.3V)
DL1, DL2 to PGND	-0.3V to (VL + 0.3V)
CKO, REF, OSC, ILIM1, ILIM2, COMP1, COMP2 to GND	-0.3V to (VL + 0.3V)
FB1, FB2, RST, SYNC, EN to GND	-0.3V to +6V
VL to GND Short Circuit	Continuous
REF to GND Short Circuit	Continuous
Operating Temperature Range	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Continuous Power Dissipation ($T_A = +70^0$)	
24-Pin QSOP	762mW
Derates above +70°C	
24-Pin QSOP	9.4mW/°C

II. Manufacturing Information

A. Description/Function: Dual 180° Out-of-Phase PWM Step-Down Controller with Power Sequencing and POR

B. Process: S8 (Standard 0.8 micron silicon gate CMOS)

C. Number of Device Transistors: 6688

D. Fabrication Location: California, USA

E. Assembly Location: Philippines, Malaysia or Thailand

F. Date of Initial Production: April, 2002

III. Packaging Information

A. Package Type: **24-Lead QSOP**

B. Lead Frame: Copper

C. Lead Finish: Solder Plate or 100% Matte Tin

D. Die Attach: Silver-filled epoxy

E. Bondwire: Gold (1.3 mil dia.)

F. Mold Material: Epoxy with silica filler

G. Assembly Diagram: Buildsheet # 05-2301-0114

H. Flammability Rating: Class UL94-V0

I. Classification of Moisture Sensitivity Per JEDEC standard J-STD-022-C: Level 1

IV. Die Information

A. Dimensions: 80 x 103 mils

B. Passivation: Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)

C. Interconnect: Aluminum/Copper/Silicon

D. Backside Metallization: None

E. Minimum Metal Width: .8 microns (as drawn)

F. Minimum Metal Spacing: .8 microns (as drawn)

G. Bondpad Dimensions: 5 mil. Sq.

H. Isolation Dielectric: SiO_2

I. Die Separation Method: Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:

Jim Pedicord (Manager, Reliability Operations)
Bryan Preeshl (Managing Director of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 231 \times 2}$$ (Chi square value for MTTF upper limit)

Thermal acceleration factor assuming a 0.8eV activation energy

$\lambda = 4.70 \times 10^{-9}$ $\lambda = 4.70$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure the reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on lots exceeding this level. The following Burn-In Schematic (Spec. #06-5831) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The PY99-2 die type has been found to have all pins able to withstand a transient pulse of ±200V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1
Reliability Evaluation Test Results

MAX1858EEG

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		231	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	QSOP	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots.
Note 2: Generic package/process data

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

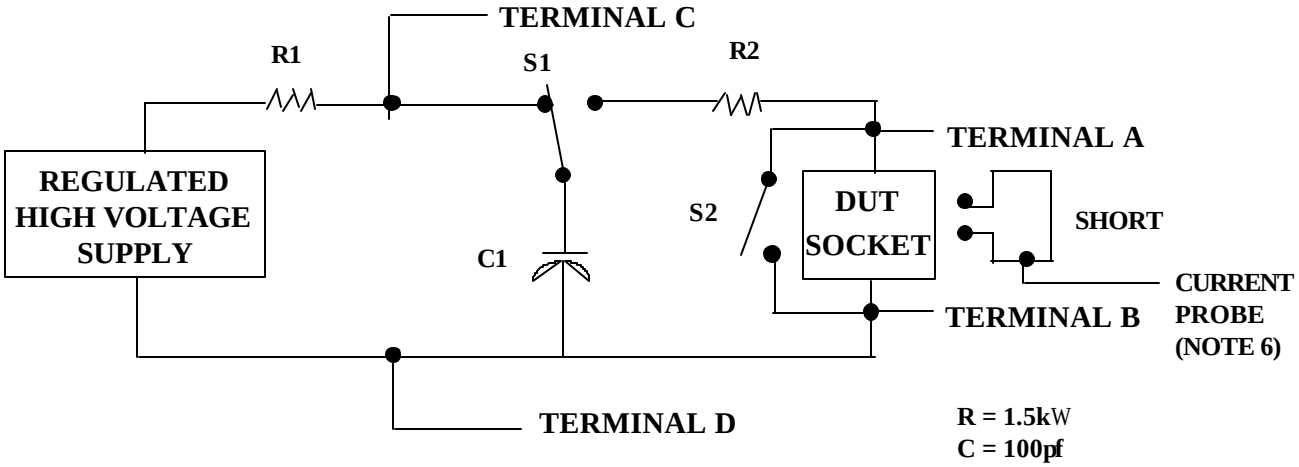
1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground (e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

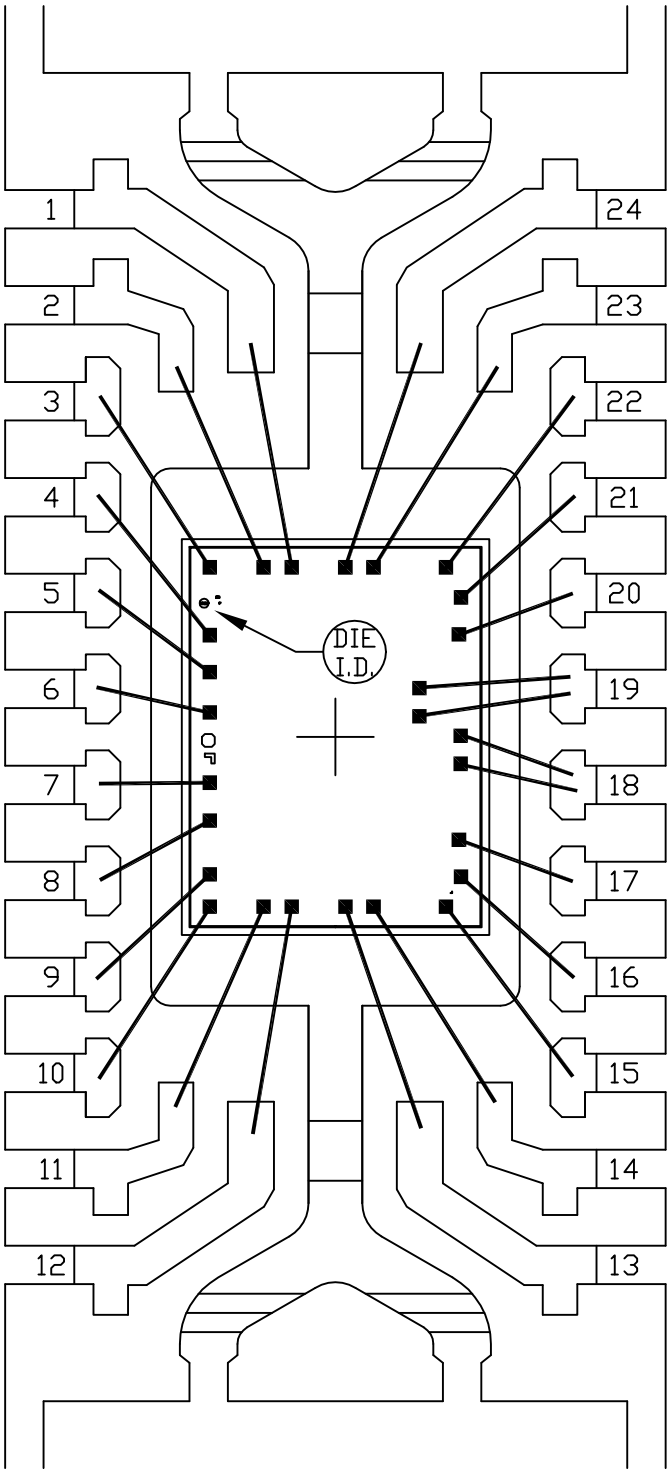
3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

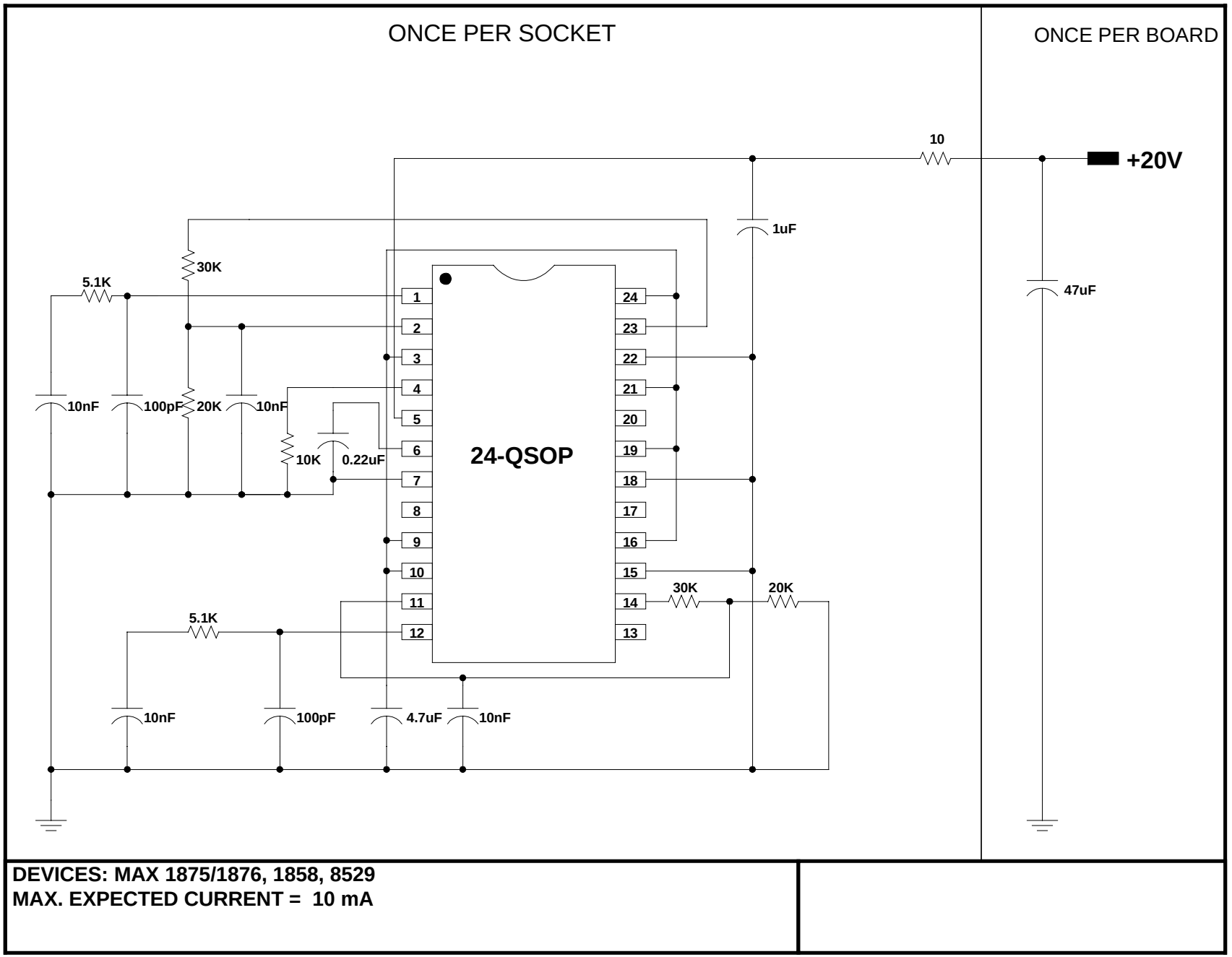
b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.





PKG. CODE: E24-1		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 96X140	PKG.			BOND DIAGRAM #: 05-2301-0114	REV: B
	DESIGN				



DEVICES: MAX 1875/1876, 1858, 8529
MAX. EXPECTED CURRENT = 10 mA