



RELIABILITY REPORT
FOR
MAX182_EWI+T / MAX182_CPI+T
PLASTIC ENCAPSULATED DEVICES

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MAXIM INTEGRATED

160 RIO ROBLES
SAN JOSE, CA 95134

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Conclusion

The MAX182_EWI+T / MAX182_CPI+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX182 is a complete, calibrated 4-channel 12-bit A/D converter (ADC) which includes a precision voltage reference, track-and-hold, and conversion clock. Internal calibration circuitry maintains true 12-bit performance over the full operating temperature range without external adjustments. In addition, each 60 μ s conversion includes an auto-zero cycle which reduces zero errors to typically below 100 μ V. CHIP SELECT, READ, and WRITE inputs are included for easy microprocessor interfacing without additional logic, 2-byte, 12-bit conversion data is provided over an 8-bit three-state output bus. Either byte may be read first. Two address bits control the 4-channel input multiplexer. The MAX182's analog input range is 0V to +5V when using a +5V reference. All four high-impedance input channels have excellent matching (typically 0.05 LSB). The MAX182A's internal reference accuracy is $\pm 0.3\%$, while the MAX182B is intended for use with an external reference.

II. Manufacturing Information

A. Description/Function:	Calibrated 4-Channel 12-Bit ADC with T/H and Reference	
B. Process:	SG5	
C. Fabrication Location:	USA	
D. Assembly Location:	Malaysia, Taiwan, Philippines, Thailand	Philippines
E. Date of Initial Production:	Pre 1997	

III. Packaging Information

A. Package Type:	28-pin SOIC (W)	28-pin PDIP
B. Lead Frame:	Copper	Copper
C. Lead Finish:	100% matte Tin	100% matte Tin
D. Bondwire:	Au (1.3 mil dia.)	Au (1.3 mil dia.)
E. Mold Material:	Epoxy with silica filler	Epoxy with silica filler
F. Assembly Diagram:	#05-0101-0199	05-0101-0198
G. Flammability Rating:	Class UL94-V0	Class UL94-V0
H. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1	Level 1
I. Single Layer Theta Ja:	80°C/W	70°C/W
J. Single Layer Theta Jc:	18°C/W	21°C/W
K. Multi Layer Theta Ja:	59°C/W	N/A°C/W
L. Multi Layer Theta Jc:	18°C/W	N/A°C/W

IV. Die Information

A. Dimensions:	134X164 mils
B. Passivation:	Si ₃ N ₄ /SiO ₂ (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Minimum Metal Width:	5.0 microns (as drawn)
E. Minimum Metal Spacing:	5.0 microns (as drawn)
F. Isolation Dielectric:	SiO ₂
G. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

- A. Quality Assurance Contacts: Eric Wright (Reliability Engineering)
Brian Standley (Manager, Reliability)
Bryan Preeshl (Vice President of QA)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% for all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 640 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 1.72 \times 10^{-9}$$

$$\lambda = 1.72 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at <http://www.maximintegrated.com/qa/reliability/monitor>. Cumulative monitor data for the SG5 Process results in a FIT Rate of 0.12 @ 25C and 2.04 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing

The AD34-3 die type has been found to have all pins able to withstand a HBM transient pulse of +/-1000V per Mil-Std 883 Method 3015.7. Latch-Up testing has shown that this device withstands a current of +/-100mA and overvoltage per JEDEC JESD78.

Table 1
Reliability Evaluation Test Results
MAX182_EWI+T / MAX182_CPI+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135C Biased Time = 192 hrs.	DC Parameters & functionality	640	0	

Note 1: Life Test Data may represent plastic DIP qualification lots.