RELIABILITY REPORT

FOR

MAX17681ATB+T

PLASTIC ENCAPSULATED DEVICES

June 10, 2016

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
Eric Wright
Quality Assurance
Reliability Engineer

Conclusion

The MAX17681ATB+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX17681 is a high-voltage, high-efficiency, iso-buck DC-DC converter designed to provide isolated power up to 3W. The device operates over a wide 4.5V to 42V input and uses primary-side feedback to regulate the output voltage. The MAX17681 uses peak-current-mode control. The low-resistance, on-chip MOSFETs ensure high efficiency at full load while simplifying the PCB layout. The device is available in a compact 10-pin (3mm x 2mm) TDFN package. Simulation models are available.

II. Manufacturing Information

A. Description/Function:	4.5V to 42V Input, High-Efficiency, Iso-Buck DC-DC Converter
B. Process:	S18
C. Number of Device Transistors:	14609
D. Fabrication Location:	USA, Japan
E. Assembly Location:	Taiwan, Thailand
F. Date of Initial Production:	September 24, 2014

III. Packaging Information

A. Package Type:	10-pin TDFN
B. Lead Frame:	Copper
C. Lead Finish:	NiPdAu
D. Die Attach:	Non-conductive
E. Bondwire:	Au (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-4357
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	87.5°C/W
K. Single Layer Theta Jc:	18.2°C/W
L. Multi Layer Theta Ja:	67.3°C/W
M. Multi Layer Theta Jc:	18.2°C/W

IV. Die Information

A. Dimensions:	40.9449X103.937 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.23 microns (as drawn)
F. Minimum Metal Spacing:	0.23 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Eric Wright (Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% for all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 80 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 13.7 \times 10^{-9}$

$\lambda = 13.7$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S18 Process results in a FIT Rate of 0.40 @ 25C and 6.96 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing

The PI01 die type has been found to have all pins able to withstand an HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-100mA and overvoltage per JEDEC JESD78

With the following exception:
EN pin passes +100mA/-10mA per JEDEC JESD78

Table 1

Reliability Evaluation Test Results

MAX17681ATB+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135C Biased Time = 192 hrs.	DC Parameters & functionality	80	0	

Note 1: Life Test Data may represent plastic DIP qualification lots.