RELIABILITY REPORT

FOR

MAX17558ATJ+T

PLASTIC ENCAPSULATED DEVICES

November 17, 2015

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
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Quality Assurance
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Conclusion

The MAX17558ATJ+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX17558 is a dual-output, synchronous step-down controller that drives nMOSFETs.

The device features a peak-current-mode, constant-frequency architecture, allowing it to operate up to 2.2MHz. The device can be configured as two single-phase, independent 10A power supplies or as a dual-phase, single-output 20A power supply. The device also provides the ability to run two controllers 180° out-of-phase to reduce the power loss and noise due to the input-capacitor ESR.

The IC supports current sensing using either an external current-sense resistor for accuracy or an inductor DCR for improved system efficiency. Current foldback limits MOSFET power dissipation under short-circuit conditions.

The IC provides independent adjustable soft-start for each output and can start up monotonically into a pre-biased output. The IC can be configured in either PWM or DCM modes of operation, depending on whether constant-frequency operation or light-load efficiency is desired.

The IC operates over the -40°C to +125°C temperature range and is available in a lead(Pb)-free, 32-pin TQFN, 5mm x 5mm package with an exposed pad.

II. Manufacturing Information

A. Description/Function:	60V, Dual-Output, Synchronous Step-Down Controller
B. Process:	S18
C. Number of Device Transistors:	65132
D. Fabrication Location:	Japan
E. Assembly Location:	Taiwan, Thailand, China
F. Date of Initial Production:	March 27, 2015

III. Packaging Information

A. Package Type:	32-pin TQFN 5x5
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Bondwire:	Au (1.3 mil dia.)
E. Mold Material:	Epoxy with silica filler
F. Assembly Diagram:	#05-9000-5812
G. Flammability Rating:	Class UL94-V0
H. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
I. Single Layer Theta Ja:	47°C/W
J. Single Layer Theta Jc:	1.7°C/W
K. Multi Layer Theta Ja:	29°C/W
L. Multi Layer Theta Jc:	1.7°C/W

IV. Die Information

A. Dimensions:	91.3386 X 106.2992 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Minimum Metal Width:	0.23 microns (as drawn)
E. Minimum Metal Spacing:	0.23 microns (as drawn)
F. Isolation Dielectric:	SiO_2
G.Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% for all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 77 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 14.28 \times 10^{-9}$

$\lambda = 14.28$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S18 Process results in a FIT Rate of 0.40 @ 25C and 6.96 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing

The PI05-1 die type has been found to have all pins able to withstand an HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-100mA and overvoltage per JEDEC JESD78.

Table 1

Reliability Evaluation Test Results

MAX17558ATJ+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135C Biased Time = 192 hrs.	DC Parameters & functionality	77	0	

Note 1: Life Test Data may represent plastic DIP qualification lots.