RELIABILITY REPORT

FOR MAX17115ETJ+

PLASTIC ENCAPSULATED DEVICES

November 16, 2009

MAXIM INTEGRATED PRODUCTS

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Conclusion

The MAX17115ETJ+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX17115 includes a high-performance step-up regulator, a high-accuracy, high-voltage, low-dropout linear regulator (LDO), a high-performance buffer amplifier, and a logic-controlled high-voltage switch block. The DC-DC converter is a high-frequency (1.2MHz/640kHz) current-mode step-up regulator with a built-in power MOSFET. It provides fast-transient response to pulsed loads while producing efficiencies over 88%. The built-in power MOSFET allows output voltages as high as 18V from inputs from 2.5V to 5.5V. A programmable soft-start function controls startup inrush currents. The operational amplifier, typically used to drive the LCD backplane (VCOM), features high-output short-circuit current (200mA), fast slew rate (45V/Fs), and wide bandwidth (20MHz). Its rail-to-rail input and output maximize application flexibility. The high-voltage LDO is adjustable and has a high accuracy of Q0.5%. It is typically used to drive a gamma reference divider string. The high-voltage switch control block modulates the shape of the gate-on supply and provides an adjustable delay for power-up sequencing. The high-voltage stress (HVS) function is used to temporarily increase the source-driver supply voltage of the LCD panel for aging tests. The HVS digital input controls an open-drain internal switch, which is typically used to change the feedback divider of the step-up regulator. The MAX17115 is available in a lead-free, 32-pin, thin QFN package. The package is a 5mm x 5mm square with a maximum thickness of 0.8mm for thin LCD panel design.

II. Manufacturing Information

A. Description/Function:	Internal-Switch Boost Regulator and High-Voltage, Low-Dropout Linear Regulator for TFT LCDs
B. Process:	S45
C. Number of Device Transistors:	9170
D. Fabrication Location:	California, Texas or Japan
E. Assembly Location:	Thailand, China
F. Date of Initial Production:	October 24, 2009

III. Packaging Information

A. Package Type:	32-pin TQFN 5x5
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-3543
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	47°C/W
K. Single Layer Theta Jc:	1.7°C/W
L. Multi Layer Theta Ja:	29°C/W
M. Multi Layer Theta Jc:	1.7°C/W

IV. Die Information

A. Dimensions:	88 X 88 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1 = 0.5 / Metal2 = 0.6 / Metal3 = 0.6 microns (as drawn)
F. Minimum Metal Spacing:	Metal1 = 0.45 / Metal2 = 0.5 / Metal3 = 0.6 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Ken Wendel (Director, Reliability Engineering) Bryan Preeshl (Managing Director of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 96 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 11.45 \times 10^{-9}$

$\lambda = 11.45$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maxim-ic.com/qa/reliability/monitor. Cumulative monitor data for the S45 Process results in a FIT Rate of 0.49 @ 25C and 8.49 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

The industry standard 85°C/85%RH or HAST testing is monitored per device process once a quarter.

C. E.S.D. and Latch-Up Testing

The PF55 die type has been found to have all pins able to withstand a HBM transient pulse of +/- 2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of 250mA and Vcc overvoltage per JEDEC JESD78.

Table 1
Reliability Evaluation Test Results

MAX17115ETJ+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	96	0
Moisture Testing (Note 2)				
HAST	Ta = 130°C RH = 85% Biased Time = 96hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data