RELIABILITY REPORT

FOR

MAX17000AETG+

PLASTIC ENCAPSULATED DEVICES

February 27, 2009

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Approved by
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Quality Assurance
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Conclusion

The MAX17000AETG+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim"s continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim"s quality and reliability standards.

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I. Device Description

A. General

The MAX17000A pulse-width modulation (PWM) controller provides a complete power solution for notebook DDR, DDR2, and DDR3 memory. It comprises a step-down controller, a source-sink LDO regulator, and a reference buffer to generate the required VDDQ, VTT, and VTTR rails. The VDDQ rail is supplied by a step-down converter using Maxim's proprietary Quick-PWM(tm) controller. The high-efficiency, constant-on-time PWM controller handles wide input/output voltage ratios (low duty-cycle applications) with ease and provides 100ns response to load transients while maintaining a relatively constant switching frequency. The Quick-PWM architecture circumvents the poor load-transient timing problems of fixed-frequency current-mode PWMs while also avoiding the problems caused by widely varying switching frequencies in conventional constant-on-time and constant-off-time PWM schemes. The controller senses the current to achieve an accurate valley current-limit protection. It is also built in with overvoltage, undervoltage, and thermal protections. The MAX17000A can be set to run in three different modes: power-efficient SKIP mode, low-noise forced-PWM mode, and standby mode to support memory in notebook computer standby operation. The switching frequency is programmable from 200kHz to 600kHz to allow small components and high efficiency. The VDDQ output voltage can be set to a preset 1.8V or 1.5V, or be adjusted from 1.0V to 2.5V by an external resistor-divider. This output has 1% accuracy over line-and-load operating range. The MAX17000A includes a ±2A source-sink LDO regulator for the memory termination VTT rail. This VTT regulator has a ±5mV deadband that either sources or sinks, ideal for the fast-changing load burst present in memory termination applications. This feature also reduces output capacitance requirements. The VTTR reference buffer sources and sinks ±3mA, providing the reference voltage needed by the memory controller and devices on the memory bus. The MAX17000A is available in a 24-pin, 4mm x 4mm, thin QFN package.

II. Manufacturing Information

A. Description/Function:	Complete DDR2 and DDR3 Memory Power-Management Solution
B. Process:	S4
C. Number of Device Transistors:	7856
D. Fabrication Location:	California
E. Assembly Location:	ASAT China, UTL Thailand, Unisem Malaysia, ISPL Philippines
F. Date of Initial Production:	October 2, 2008

III. Packaging Information

A. Package Type:	24-pin TQFN 4x4
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive Epoxy
E. Bondwire:	Au (2.0 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	48°C/W
K. Single Layer Theta Jc:	2.7°C/W
L. Multi Layer Theta Ja:	36°C/W
M. Multi Layer Theta Jc:	2.7°C/W

IV. Die Information

A. Dimensions:	74 X 70 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1 = 0.5 / Metal2 = 0.6 / Metal3 = 0.6 microns (as drawn)
F. Minimum Metal Spacing:	Metal1 = 0.45 / Metal2 = 0.5 / Metal3 = 0.6 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Ken Wendel (Director, Reliability Engineering) Bryan Preeshl (Managing Director of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 48 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 22.4 \times 10^{-9}$

$\lambda = 22.4$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly 1000 hour life test monitors on its processes. This data is published in the Product Reliability Report found at http://www.maxim-ic.com/. Current monitor data for the S4 Process results in a FIT Rate of 0.28 @ 25C and 4.85 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

The industry standard 85°C/85%RH or HAST testing is monitored per device process once a quarter.

C. E.S.D. and Latch-Up Testing

The PE07-1 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2000 V per JEDEC JESD22-A114-D. Latch-Up testing has shown that this device withstands a current of +/-250 mA, 1.5x VCCMax Overvoltage per JESD78.

Table 1
Reliability Evaluation Test Results

MAX17000AETG+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	48	0
Moisture Testing (Note 2)				
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data