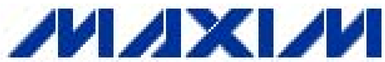

RELIABILITY REPORT

FOR MAX16068ETI+

PLASTIC ENCAPSULATED DEVICES

September 14, 2010

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Approved by
Richard Aburano
Quality Assurance
Manager, Reliability Operations

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Conclusion

The MAX16068ETI+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX16068 flash-configurable system manager monitors and manages up to six system voltages simultaneously. The MAX16068 integrates an analog-to-digital converter (ADC). Device configuration information, including overvoltage and undervoltage limits, time delay settings is stored in nonvolatile flash memory. During a fault condition, fault flags and channel voltages can be automatically stored in the nonvolatile flash memory for later readback. The internal 1% accurate, 10-bit ADC measures each input and compares the result to one overvoltage and one undervoltage limit. A fault signal asserts when a monitored voltage falls outside the set limits. The MAX16068 supports a power-supply voltage of up to 14V and can be powered directly from the 12V intermediate bus in many systems. The MAX16068 includes six programmable general-purpose inputs/outputs (GPIOs). GPIOs are flash configurable as a fault output, as a watchdog input or output, or as a manual reset. The MAX16068 features nonvolatile fault memory for recording information during system shutdown events. The fault logger records a failure in the internal flash and sets a lock bit protecting the stored fault data from accidental erasure. An SMBus(tm) or a JTAG serial interface configures the MAX16068. The MAX16068 is available in a 28-pin, 5mm × 5mm, TQFN package and is fully specified over the -40°C to +85°C extended temperature range.

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II. Manufacturing Information

A. Description/Function:	6-Channel, Flash-Configurable System Manager with Nonvolatile Fault Registers
B. Process:	S4
C. Number of Device Transistors:	112745
D. Fabrication Location:	California, Texas or Japan
E. Assembly Location:	China, Malaysia and Thailand
F. Date of Initial Production:	October 24, 2009

III. Packaging Information

A. Package Type:	28-pin TQFN 5x5
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-3942
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	47°C/W
K. Single Layer Theta Jc:	2.1°C/W
L. Multi Layer Theta Ja:	29°C/W
M. Multi Layer Theta Jc:	2.1°C/W

IV. Die Information

A. Dimensions:	101 X 91 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1 = 0.5 / Metal2 = 0.6 / Metal3 = 0.6 microns (as drawn)
F. Minimum Metal Spacing:	Metal1 = 0.45 / Metal2 = 0.5 / Metal3 = 0.6 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

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V. Quality Assurance Information

A. Quality Assurance Contacts: Richard Aburano (Manager, Reliability Operations)
Bryan Preeshl (Managing Director of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 48 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 22.9 \times 10^{-9}$

λ = 22.9 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maxim-ic.com/qa/reliability/monitor. Cumulative monitor data for the S4 Process results in a FIT Rate of 0.05 @ 25C and 0.83 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot EXLZAQ001F, D/C 0941)

The MT17 die type has been found to have all pins able to withstand a HBM transient pulse of +/- 2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/- 250mA and overvoltage per JEDEC JESD78.

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Table 1

Reliability Evaluation Test Results

MAX16068ETI+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	48	0	EXLZAQ001G, D/C 0940

Note 1: Life Test Data may represent plastic DIP qualification lots.

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