RELIABILITY REPORT

FOR

MAX16066ETL+

PLASTIC ENCAPSULATED DEVICES

June 10, 2013

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
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Quality Assurance
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Conclusion

The MAX16066ETL+ successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX16065/MAX16066 flash-configurable system managers monitor and sequence multiple system voltages. The MAX16065/MAX16066 can also accurately monitor (±2.5%) one current channel using a dedicated high-side current-sense amplifier. The MAX16065 manages up to twelve system voltages simultaneously, and the MAX16066 manages up to eight supply voltages. These devices integrate a selectable differential or single-ended analog-to-digital converter (ADC) and configurable outputs for sequencing power supplies. Device configuration information, including overvoltage and undervoltage limits, timing settings, and the sequencing order is stored in nonvolatile flash memory. During a fault condition, fault flags and channel voltages can be automatically stored in the nonvolatile flash memory for later read-back. The internal 1% accurate 10-bit ADC measures each input and compares the result to one overvoltage, one undervoltage, and one early warning limit that can be configured as either undervoltage or overvoltage. A fault signal asserts when a monitored voltage falls outside the set limits. Up to three independent fault output signals are configurable to assert under various fault conditions. Because the MAX16065/MAX16066 support a power-supply voltage of up to 14V, they can be powered directly from the 12V intermediate bus in many systems. The integrated sequencer provides precise control over the power-up and power-down order of up to twelve (MAX16065) or up to eight (MAX16066) power supplies. Eight outputs (EN_OUT1-EN_OUT8) are configurable with charge-pump outputs to directly drive external n-channel MOSFETs. The MAX16065/MAX16066 include eight/six programmable general-purpose inputs/outputs (GPIO_s). GPIO_s are flash configurable as dedicated fault outputs, as a watchdog input or output, or as a manual reset. The MAX16065/MAX16066 feature nonvolatile fault memory for recording information during system shutdown events. The fault logger records a failure in the internal flash and sets a lock bit protecting the stored fault data from accidental erasure. An SMBus or a JTAG serial interface configures the MAX16065/MAX16066. The MAX16065 is available in a 48-pin, 7mm x 7mm, TQFN package, and the MAX16066 is available in a 40-pin, 6mm x 6mm, TQFN package. Both devices are fully specified from -40°C to +85°C.

II. Manufacturing Information

A. Description/Function:	12-Channel/8-Channel Flash-Configurable System Managers with Nonvolatile Fault Registers
B. Process:	S4
C. Number of Device Transistors:	181965
D. Fabrication Location:	California, Texas, or Japan
E. Assembly Location:	China or Thailand
F. Date of Initial Production:	July 17, 2009

III. Packaging Information

A. Package Type:	40-pin TQFN 6x6
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-3545
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	38°C/W
K. Single Layer Theta Jc:	1.4°C/W
L. Multi Layer Theta Ja:	27°C/W
M. Multi Layer Theta Jc:	1.4°C/W

IV. Die Information

A. Dimensions:	121X114 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1 = 0.5 microns (as drawn)
F. Minimum Metal Spacing:	Metal1 = 0.45 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Richard Aburano (Manager, Reliability Engineering) Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 48 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 22.9 \times 10^{-9}$

$\lambda = 22.9$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S4 Process results in a FIT Rate of 0.13 @ 25C and 2.31 @ 55C (0.8 eV, 60% UCL).

B. E.S.D. and Latch-Up Testing (ESD lot EAGS5A005D D/C 1244, Latch-Up lot STZZCQ001D D/C 0921)

The MT16 die type has been found to have all pins able to withstand a HBM transient pulse of +/-1500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA and overvoltage per JEDEC JESD78.

Table 1
Reliability Evaluation Test Results

MAX16066ETL+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	48	0	STZZCQ001D, D/C 0921

Note 1: Life Test Data may represent plastic DIP qualification lots.