

RELIABILITY REPORT FOR MAX16039 PLASTIC ENCAPSULATED DEVICES

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MAXIM INTEGRATED PRODUCTS

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Conclusion

The MAX16039 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX16033-MAX16040 supervisory circuits reduce the complexity and number of components required for power-supply monitoring and battery control functions in microprocessor (μP) systems. The devices significantly improve system reliability and accuracy compared to other ICs or discrete components. The MAX16033-MAX16040 provide μP reset, backup-battery switchover, power-fail warning, watchdog, and chip-enable gating features. The MAX16033-MAX16040 operate from supply voltages up to 5.5V. The factory-set reset threshold voltage ranges from 2.32V to 4.63V. The devices feature a manual-reset input (MAX16033/MAX16037), a watchdog timer input (MAX16034/MAX16038), a battery-on output (MAX16035/MAX16039), an auxiliary adjustable reset input (MAX16036/MAX16040), and chip-enable gating (MAX16033-MAX16036). Each device includes a power-fail comparator and offers an active-low push-pull reset or an active-low open-drain reset. The MAX16033-MAX16040 are available in 2mm x 2mm, 8-pin or 10-pin μDFN packages and are fully specified from -40°C to +85°C.



II. Manufacturing Information

A. Description/Function: Low-Power Battery Backup Circuits in Small µDFN Packages

B. Process: B8

C. Number of Device Transistors:

D. Fabrication Location: California or Texas

E. Assembly Location: ThailandF. Date of Initial Production: July 28, 2007

III. Packaging Information

A. Package Type: 8-pin uDFN
B. Lead Frame: Substrate
C. Lead Finish: Gold

D. Die Attach: Non-conductive
E. Bondwire: Au (1 mil dia.)
F. Mold Material: Epoxy with silica filler
G. Assembly Diagram: #05-9000-2616
H. Flammability Rating: Class UL94-V0

I. Classification of Moisture Sensitivity per Level 1

JEDEC standard J-STD-020-C

J. Single Layer Theta Ja:

K. Single Layer Theta Jc:

C/W

K. Multi Layer Theta Ja:

M. Multi Layer Theta Jc:

122.1°C/W

IV. Die Information

A. Dimensions: 62 X 45 mils

B. Passivation: Si₃N₄/SiO₂ (Silicon nitride/ Silicon dioxide)

C. Interconnect: Al/0.5%Cu with Ti/TiN Barrier

D. Backside Metallization: None

E. Minimum Metal Width: 0.8 microns (as drawn)F. Minimum Metal Spacing: 0.8 microns (as drawn)

G. Bondpad Dimensions: 5 mil. Sq.
 H. Isolation Dielectric: SiO₂
 I. Die Separation Method: Wafer Saw



V. Quality Assurance Information

A. Quality Assurance Contacts: Richard Aburano (Manager, Reliability Operations)

Bryan Preeshl (Managing Director of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.

0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppmD. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maxim-ic.com/qa/reliability/monitor. Cumulative monitor data for the B8 Process results in a FIT Rate of 0.06 @ 25C and 0.99 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot TDIVBQ002B, D/C 0820)

The MT05-4 die type has been found to have all pins able to withstand a HBM transient pulse of +/- 2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/- 250mA and overvoltage per JEDEC JESD78.