RELIABILITY REPORT

FOR

MAX16021LTES+
(MAX16016/MAX16020/MAX16021)

PLASTIC ENCAPSULATED DEVICES

December 2, 2008

**MAXIM INTEGRATED PRODUCTS**

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

| **Approved by** |
|---|
| Ken Wendel |
| Quality Assurance |
| Director, Reliability Engineering |

**Conclusion**

The MAX16021LTES+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim"s continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim"s quality and reliability standards.

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**I. Device Description**

A. General

The MAX16016/MAX16020/MAX16021 supervisory circuits monitor power supplies, provide battery-backup control, and chip-enable (CE) gating to write protect memory in microprocessor (µP)-based systems. These low-power devices improve system reliability by providing several supervisory functions in a small, single integrated solution. The MAX16016/MAX16020/MAX16021 perform four basic system functions: Provide a µP reset output during VCC supply powerup, power-down, and brownout conditions. Control VCC to battery-backup switching internally to maintain data or low-power operation for memories, real-time clocks (RTCs), and other digital logic when the main power is removed. Provide memory write protection through internal chip-enable gating during brownout. Provide a combination of additional supervisory functions listed in the Features section in the full data sheet. The MAX16016/MAX16020/MAX16021 operate from a 1.53V to 5.5V supply voltage and offer fixed reset thresholds for monitoring 5V, 3.3V, 3V, 2.5V, and 1.8V systems. Each device is available with either a pushpull or open-drain reset output. The MAX16016/MAX16020/MAX16021 are available in small TDFN/TQFN packages and are fully specified for an operating temperature range of -40°C to +85°C.

## II. Manufacturing Information

| | |
|---|---|
| A. Description/Function: | Low-Power ìP Supervisory Circuits with Battery-Backup Circuit and Chip-Enable Gating |
| B. Process: | B8 |
| C. Number of Device Transistors: | |
| D. Fabrication Location: | Texas |
| E. Assembly Location: | ASAT China, UTL Thailand |
| F. Date of Initial Production: | 9/29/2008 |

## III. Packaging Information

| | |
|---|---|
| A. Package Type: | 16-pin TQFN 4x4 |
| B. Lead Frame: | Copper |
| C. Lead Finish: | 100% matte Tin |
| D. Die Attach: | Conductive Epoxy |
| E. Bondwire: | Au (1.0 mil dia.) |
| F. Mold Material: | Epoxy with silica filler |
| G. Assembly Diagram: | # |
| H. Flammability Rating: | Class UL94-V0 |
| I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C | Level 1 |
| J. Single Layer Theta Ja: | 59.3°C/W |
| K. Single Layer Theta Jc: | 5.7°C/W |
| L. Multi Layer Theta Ja: | 40°C/W |
| M. Multi Layer Theta Jc: | 5.7°C/W |

## IV. Die Information

| | |
|---|---|
| A. Dimensions: | 63 X 88 mils |
| B. Passivation: | $Si_3N_4/SiO_2$ (Silicon nitride/ Silicon dioxide |
| C. Interconnect: | Aluminum/Si (Si = 1%) |
| D. Backside Metallization: | None |
| E. Minimum Metal Width: | 0.8 microns (as drawn) |
| F. Minimum Metal Spacing: | 0.8 microns (as drawn) |
| G. Bondpad Dimensions: | 5 mil. Sq. |
| H. Isolation Dielectric: | $SiO_2$ |
| I. Die Separation Method: | Wafer Saw |

## V. Quality Assurance Information

| | |
|---|---|
| A. Quality Assurance Contacts: | Ken Wendel (Director, Reliability Engineering)<br>Bryan Preeshl (Managing Director of QA) |
| B. Outgoing Inspection Level: | 0.1% for all electrical parameters guaranteed by the Datasheet.<br>0.1% For all Visual Defects. |
| C. Observed Outgoing Defect Rate: | < 50 ppm |
| D. Sampling Plan: | Mil-Std-105D |

## VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are pending. Using these results, the Failure Rate ($\lambda$) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 96 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 11.2 \times 10^{-9}$

$\lambda$ = 11.2 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly 1000 hour life test monitors on its processes. This data is published in the Product Reliability Report found at http://www.maxim-ic.com/. Current monitor data for the B8 Process results in a FIT Rate of 2.71 @ 25C and 17.30 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

The industry standard 85°C/85%RH or HAST testing is monitored per device process once a quarter.

C. E.S.D. and Latch-Up Testing

The MS98 die type has been found to have all pins able to withstand a HBM transient pulse of +/-1500 V per JEDEC JESD22-A114-D. Latch-Up testing per JESD78 has shown that this device withstands an I-Test of +/-250mA and a V-Test of +/-1.5 VccMax.

**Table 1**
Reliability Evaluation Test Results

**MAX16021LTES+**

| TEST ITEM | TEST CONDITION | FAILURE IDENTIFICATION | SAMPLE SIZE | NUMBER OF FAILURES |
|---|---|---|---|---|
| **Static Life Test** (Note 1) | | | | |
| | Ta = 135°C<br>Biased<br>Time = 192 hrs. | DC Parameters & functionality | 96 | 0 |
| **Moisture Testing** (Note 2) | | | | |
| 85/85 | Ta = 85°C<br>RH = 85%<br>Biased<br>Time = 1000hrs. | DC Parameters & functionality | 77 | 0 |
| **Mechanical Stress** (Note 2) | | | | |
| Temperature Cycle | -65°C/150°C<br>1000 Cycles<br>Method 1010 | DC Parameters & functionality | 77 | 0 |

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data