

RELIABILITY REPORT
FOR
MAX1567ETL
PLASTIC ENCAPSULATED DEVICES

November 13, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

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Conclusion

The MAX1567 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX1567 provides a complete power-supply solution for digital cameras. It improves performance, component count, and size compared to conventional multichannel controllers in 2-cell AA, 1-cell lithium-ion (Li+), and dual-battery designs. On-chip MOSFETs provide up to 95% efficiency for critical power supplies, while additional channels operate with external FETs for optimum design flexibility. This optimizes overall efficiency and cost, while also reducing board space.

The MAX1567 includes six high-efficiency DC-to-DC conversion channels:

- Step-up DC-to-DC converter with on-chip power FETs
- Main DC-to-DC converter with on-chip FETs, configurable to step **either** up or down
- Step-down core DC-to-DC converter with on-chip FETs
- DC-to-DC controller for white LEDs or other output
- Transformerless inverting DC-to-DC controller (typically for negative CCD bias)

All DC-to-DC channels operate at one fixed frequency settable from 100kHz to 1MHz to optimize size, cost, and efficiency. Other features include soft-start, power-OK outputs, and overload protection. The MAX1567 is available in space-saving 40-pin thin QFN packages. An evaluation kit is available to expedite designs.

B. Absolute Maximum Ratings

| <u>Item</u> | <u>Rating</u> |
|--|-------------------------|
| PV, PVSU, SDOK, AUX10K, SCF, ON_, FB_, SUSU to GND | -0.3V to +6V |
| PG_ to GND | -0.3V to +0.3V |
| DL1, DL3, INDL2, PVM, PVSD to GND | -0.3V to (PVSU + 0.3V) |
| DL2 to GND | -0.3V to (INDL2 + 0.3V) |
| LXSU Current (Note 1) | 3.6A |
| LXM Current (Note 1) | 3.6A |
| LXSD Current (Note 1) | 2.25A |
| REF, OSC, CC_ to GND | -0.3V to (PVSU + 0.3V) |
| Operating Temperature Range | -40°C to +85°C |
| Junction Temperature | +150°C |
| Storage Temperature Range | -65°C to +150°C |
| Lead Temperature (soldering, 10s) | +300°C |
| Continuous Power Dissipation (TA = +70°C) | |
| 40-Pin Thin QFN | 2105mW |
| Derates above +70°C | |
| 40-Pin Thin QFN | 26.3mW/°C |

Note 1: LXSU has internal clamp diodes to PVSU and PGSU, LXM has internal clamp diodes to PVM and PGM, and LXSD has internal clamp diodes to PVSD and PGSD. Applications that forward bias these diodes should take care not to exceed the devices' power dissipation limits.

II. Manufacturing Information

| | |
|----------------------------------|---|
| A. Description/Function: | Six-Channel, High-Efficiency, Digital Camera Power Supplies |
| B. Process: | B8 (Standard 0.8 micron silicon gate CMOS) |
| C. Number of Device Transistors: | 9420 |
| D. Fabrication Location: | California, USA |
| E. Assembly Location: | Thailand |
| F. Date of Initial Production: | July, 2003 |

III. Packaging Information

| | |
|---|---------------------------------|
| A. Package Type: | 40-Lead Thin QFN (6 x 6) |
| B. Lead Frame: | Copper |
| C. Lead Finish: | Solder Plate |
| D. Die Attach: | Silver-Filled Epoxy |
| E. Bondwire: | Gold (1.3 mil dia.) |
| F. Mold Material: | Epoxy with silica filler |
| G. Assembly Diagram: | # 05-9000-0520 |
| H. Flammability Rating: | Class UL94-V0 |
| I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112: | Level 1 |

IV. Die Information

| | |
|----------------------------|---|
| A. Dimensions: | 127 x 147 mils |
| B. Passivation: | Si ₃ N ₄ /SiO ₂ (Silicon nitride/ Silicon dioxide) |
| C. Interconnect: | Aluminum/Copper/Silicon |
| D. Backside Metallization: | None |
| E. Minimum Metal Width: | .8 microns (as drawn) |
| F. Minimum Metal Spacing: | .8 microns (as drawn) |
| G. Bondpad Dimensions: | 5 mil. Sq. |
| H. Isolation Dielectric: | SiO ₂ |
| I. Die Separation Method: | Wafer Saw |

V. Quality Assurance Information

A. Quality Assurance Contacts:

Jim Pedicord (Manager, Rel Oprations)
Bryan Preeshl (Executive Director of QA)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4389 \times 48 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

└ Thermal acceleration factor assuming a 0.8eV activation energy

$$\lambda = 22.62 \times 10^{-9} \quad \lambda = 22.62 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure the reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on lots exceeding this level. The following Burn-In Schematic (Spec. #06-6202) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The PN07-1 die type has been found to have all pins able to withstand a transient pulse of +/-800V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of $\pm 250\text{mA}$.

Table 1
Reliability Evaluation Test Results

MAX1567ETL

| TEST ITEM | TEST CONDITION | FAILURE IDENTIFICATION | SAMPLE SIZE | NUMBER OF FAILURES |
|-----------------------------------|---|----------------------------------|--------------------|---------------------------|
| Static Life Test (Note 1) | | | | |
| | Ta = 135°C Biased Time = 192 hrs. | DC Parameters & functionality | 48 | 0 |
| Moisture Testing (Note 2) | | | | |
| Pressure Pot | Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs. | DC Parameters & functionality | 77 | 0 |
| 85/85 | Ta = 85°C RH = 85% Biased Time = 1000hrs. | DC Parameters & functionality | 77 | 0 |
| Mechanical Stress (Note 2) | | | | |
| Temperature Cycle | -65°C/150°C 1000 Cycles Method 1010 | DC Parameters & functionality | 77 | 0 |

Note 1: Life Test Data may represent plastic D.I.P. qualification lots.

Note 2: Generic package/process data

Attachment #1

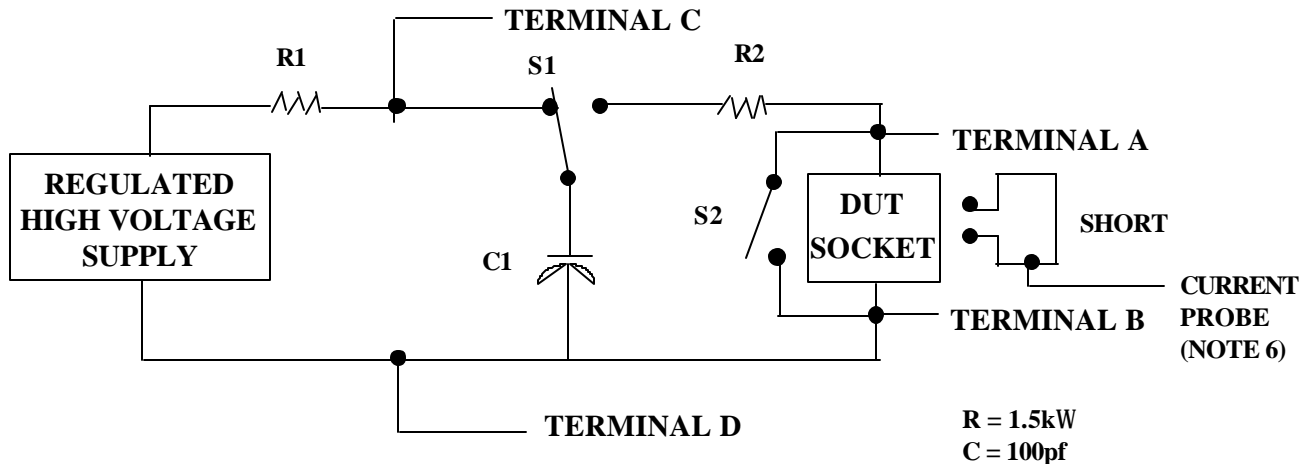
TABLE II. Pin combination to be tested. 1/ 2/

| | Terminal A (Each pin individually connected to terminal A with the other floating) | Terminal B (The common combination of all like-named pins connected to terminal B) |
|----|---|---|
| 1. | All pins except V_{PS1} 3/ | All V_{PS1} pins |
| 2. | All input and output pins | All other input-output pins |

- 1/ Table II is restated in narrative form in 3.4 below.
- 2/ No connects are not to be tested.
- 3/ Repeat pin combination I for each named Power supply and for ground (e.g., where V_{PS1} is V_{DD} , V_{CC} , V_{SS} , V_{BB} , GND, $+V_S$, $-V_S$, V_{REF} , etc).

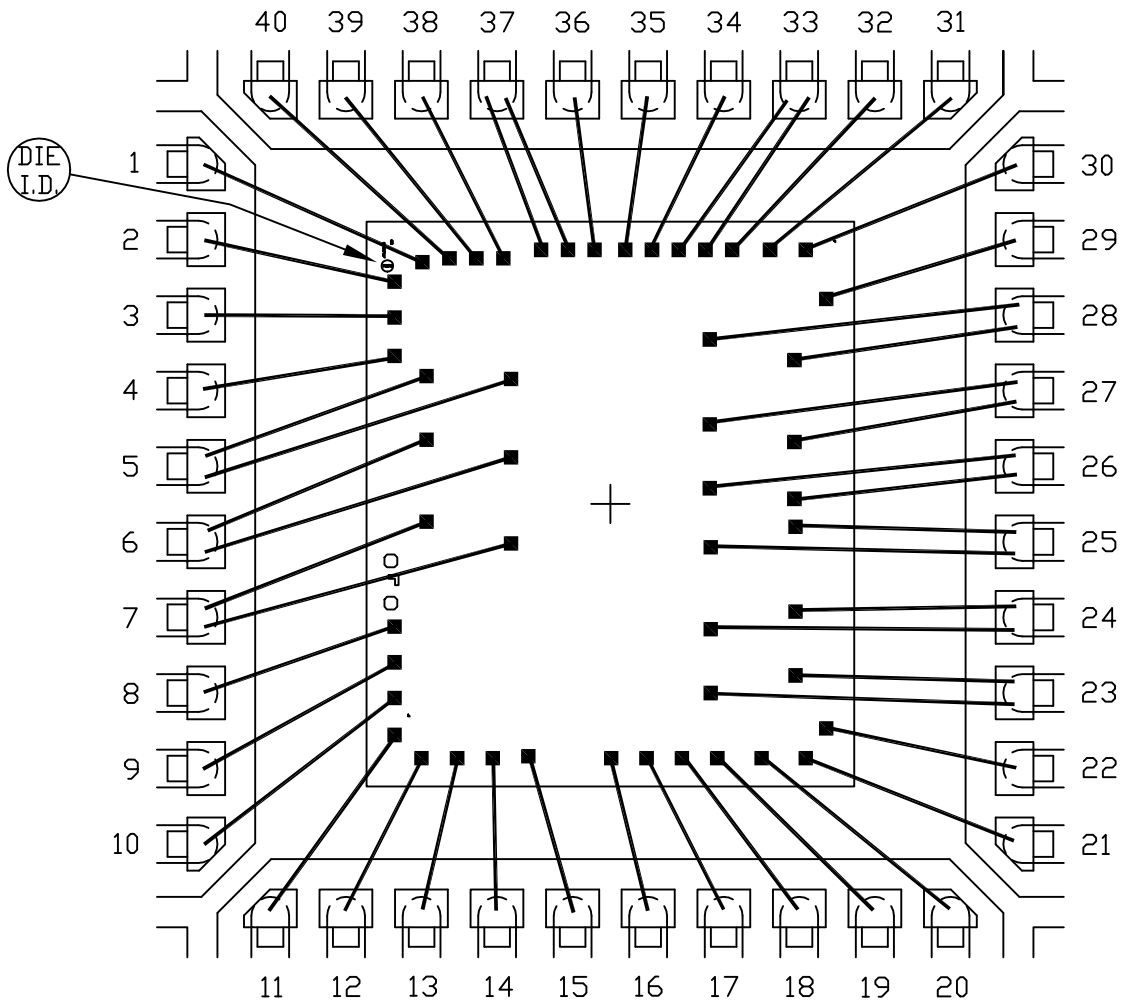
3.4 Pin combinations to be tested.

- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1} , or V_{SS2} or V_{SS3} or V_{CC1} , or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open



6x6x0.8mm QFN THIN PKG.

EXPOSED PAD PKG.



| | | | | | |
|---------------------------|----------------|------------|------|---|-----------|
| PKG. CODE: T4066-1 | | SIGNATURES | DATE |  CONFIDENTIAL & PROPRIETARY | |
| CAV./PAD SIZE: 185x185 | PKG. DESIGN | | | BOND DIAGRAM #: 05-9000-0520 | REV: A |

