RELIABILITY REPORT

FOR

MAX15090EWI+T / MAX15090AEWI+T

WAFER LEVEL DEVICES

October 3, 2015

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
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Conclusion

The MAX15090EWI+T / MAX15090AEWI+T successfully met the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX15090/MAX15090A ICs are integrated solutions for hot-swap applications requiring the safe insertion and removal of circuit line cards from a live backplane. The devices integrate a hot-swap controller, 6mω power MOSFET, and an electronic circuit-breaker protection in a single package. The devices integrate an accurate current-sense circuitry and provide 220FA/A of proportional output current. The devices are designed for protection of 2.7V to 18V supply voltages. These devices implement a foldback current limit during startup to control inrush current lowering di/dt and keep the MOSFET operating under safe operating area (SOA) conditions. After the startup cycle is complete, on-chip comparators provide variableSpeed/BiLevelK protection against short-circuit and overcurrent faults, and immunity against system noise and load transients. The load is disconnected in the event of a fault condition. The devices are factory calibrated to deliver accurate overcurrent protection with Q10% accuracy. During a fault condition, the MAX15090 latches off, while the MAX15090A enters autoretry mode. The devices feature an IN to OUT short-circuit detection before startup. The devices provide a power-MOSFET GATE pin to program the slew rate during startup by adding an external capacitor. The devices have overvoltage/ undervoltage input pins that can detect an overvoltage/ undervoltage fault and disconnect the IN from the OUT. Additional features include internal overtemperature protection, power-good output, and fault-indicator output. The MAX15090/MAX15090A are available in a 28-bump, 2.07mm x 3.53mm, power wafer-level package (WLP) and are rated over the -40°C to +85°C extended temperature range.

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II. Manufacturing Information

A. Description/Function:	MAX15090/MAX15090A 2.7V to 18V, 12A, Hot-Swap Solution with Current Report Output
B. Process:	S18
C. Number of Device Transistors:	11259
D. Fabrication Location:	USA
E. Assembly Location:	Japan
F. Date of Initial Production:	September 29, 2012

III. Packaging Information

A. Package Type:	28-bump WLP HC
B. Lead Frame:	N/A
C. Lead Finish:	N/A
D. Die Attach:	None
E. Bondwire:	N/A (N/A mil dia.)
F. Mold Material:	None
G. Assembly Diagram:	#05-9000-5023
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	N/A°C/W
K. Single Layer Theta Jc:	N/A°C/W
L. Multi Layer Theta Ja:	42°C/W
M. Multi Layer Theta Jc:	7°C/W

IV. Die Information

A. Dimensions:	140.1574 X 82.6771 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.23 microns (as drawn)
F. Minimum Metal Spacing:	0.23 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

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V. Quality Assurance Information

A. Quality Assurance Contacts: Don Lipps (Manager, Reliability Engineering)
Bryan Preeshl (Vice President of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% for all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 80 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 13.7 \times 10^{-9}$

λ = 13.7 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S18 Process results in a FIT Rate of 0.40 @ 25°C and 6.96 @ 55°C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing

The NQ90-0 die type has been found to have all pins able to withstand a transient pulse of:

ESD-HBM: +/- 2500V per JEDEC JESD22-A114

ESD-CDM: +/- 750V per JEDEC JESD22-C101

Latch-Up testing has shown that this device withstands a current of +/-100mA and overvoltage per JEDEC JESD78.

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Table 1
Reliability Evaluation Test Results

MAX15090EWI+T / MAX15090AEWI+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	80	0	

Note 1: Life Test Data may represent plastic DIP qualification lots.

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