RELIABILITY REPORT

FOR

MAX15029ATB+T

PLASTIC ENCAPSULATED DEVICES

June 21, 2013

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
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Quality Assurance
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Conclusion

The MAX15029ATB+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX15029/MAX15030 low-dropout linear regulators operate from input voltages as low as 1.425V and deliver up to 500mA of continuous output current with a typical dropout voltage of only 40mV. The output voltage is adjustable from 0.5V to VIN and is ±2% accurate over load and line variations, from -40°C to +125°C. The MAX15030 features a BIAS input of 3V to 5.5V from an always-on power supply. The BIAS input current is reduced down to less than 2µA during the shutdown. These regulators use small, 1µF ceramic input capacitors and 2.2µF ceramic output capacitors to deliver 500mA output current. High bandwidth provides excellent transient response and limits the output voltage deviation to 10mV for a 100mA to 500mA load step, with only a 2.2µF ceramic output capacitor, and the voltage deviations can be reduced further by increasing the output capacitor. These devices offer a logic-controlled shutdown input to reduce input current (IIN) consumption down to less than 5.5µA in standby mode. Other features include a soft-start to reduce inrush current, short-circuit protection, and thermal-overload protection. The MAX15030 features a BIAS input allowing a secondary supply to keep the LDO's internal circuitry alive if the voltage on IN goes to 0. Both devices are fully specified from -40°C to +125°C and are available in a 10-pin thermally enhanced TDFN package (3mm x 3mm) that includes an exposed pad for optimal power dissipation. For a 1A version of these LDOs, refer to the MAX15027/MAX15028 data sheet.

II. Manufacturing Information

A. Description/Function:	1.425V to 3.6V Input, 500mA Low-Dropout Regulators with BIAS Input
B. Process:	S4
C. Number of Device Transistors:	2664
D. Fabrication Location:	California, Texas or Japan
E. Assembly Location:	Taiwan, China, or Thailand
F. Date of Initial Production:	April 6, 2009

III. Packaging Information

A. Package Type:	10-pin TDFN 3x3
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-2981
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	54°C/W
K. Single Layer Theta Jc:	8.5°C/W
L. Multi Layer Theta Ja:	41°C/W
M. Multi Layer Theta Jc:	8.5°C/W

IV. Die Information

A. Dimensions:	46 X 72 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1 = 0.5 microns (as drawn)
F. Minimum Metal Spacing:	Metal1 = 0.45 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Richard Aburano (Manager, Reliability Engineering) Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{1000 \times 4340 \times 79 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 2.7 \times 10^{-9}$

$\lambda = 2.7$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S4 Process results in a FIT Rate of 0.13 @ 25C and 2.31 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot TJXXDQ001U D/C 1130)

The NQ10 die type has been found to have all pins able to withstand a transient pulse of:

ESD-HBM:	+/- 2500V per JEDEC JESD22-A114
ESD-CDM:	+/-750V per JEDEC JESD22-C101
ESD-MM:	+/-150V per JEDEC JESD22/A115

Latch-Up testing has shown that this device withstands a current of +/-250mA and overvoltage per JEDEC JESD78.

Table 1
Reliability Evaluation Test Results

MAX15029ATB+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135°C Biased Time = 1000 hrs.	DC Parameters & functionality	79	0	TJXXDQ001U, D/C 1130

Note 1: Life Test Data may represent plastic DIP qualification lots.