RELIABILITY REPORT

FOR

MAX15012xASA+T

PLASTIC ENCAPSULATED DEVICES

June 24, 2013

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
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Conclusion

The MAX15012xASA+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

Table of Contents

I. ....Device Description **IV. ....Die Information**

II. ....Manufacturing Information **V. ....Quality Assurance Information**

III. ....Packaging Information **VI. ....Reliability Evaluation**

.....Attachments

I. Device Description

A. General

The MAX15012/MAX15013 high-frequency, 175V half-bridge, n-channel MOSFET drivers drive high- and low-side MOSFETs in high-voltage applications. These drivers are independently controlled and their 35ns typical propagation delay, from input to output, are matched to within 2ns (typ). The high-voltage operation with very low and matched propagation delay between drivers, and high source/sink current capabilities make these devices suitable for the high-power, high-frequency telecom power converters. A reliable on-chip bootstrap diode connected between VDD and BST eliminates the need for an external discrete diode. The MAX15012A/C and MAX15013A/C offer both noninverting drivers (see the *Selector Guide* of the full data sheet). The MAX15012B/D and MAX15013B/D offer a noninverting high-side driver and an inverting low-side driver. The MAX15012A/B/C/D feature CMOS (VDD/2) logic inputs. The MAX15013A/B/C/D feature TTL logic inputs. The drivers are available in the industry-standard 8-pin SO footprint and pin configuration and a thermally enhanced 8-pin SO package. All devices operate over the -40°C to +125°C automotive temperature range.

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II. Manufacturing Information

A. Description/Function:	175V/2A, High-Speed, Half-Bridge MOSFET Drivers	
B. Process:	BCD250	
C. Number of Device Transistors:	2996	
D. Fabrication Location:	USA	
E. Assembly Location:	Thailand, Philippines, Malaysia	Philippines, Thailand
F. Date of Initial Production:	April 22, 2006	

III. Packaging Information

A. Package Type:	8-pin SOIC (N)	8-pin SOIC (N) with exposed pad
B. Lead Frame:	Copper	Copper
C. Lead Finish:	100% matte Tin	100% matte Tin
D. Die Attach:	Conductive	Conductive
E. Bondwire:	Au (1 mil dia.)	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-1069	#05-9000-1069
H. Flammability Rating:	Class UL94-V0	#05-9000-1069
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1	Level 1
J. Single Layer Theta Ja:	170°C/W	52°C/W
K. Single Layer Theta Jc:	40°C/W	6°C/W
L. Multi Layer Theta Ja:	128.4°C/W	41°C/W
M. Multi Layer Theta Jc:	36°C/W	7°C/W

IV. Die Information

A. Dimensions:	88 X 85 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiWN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	1 micron (as drawn)
F. Minimum Metal Spacing:	2 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

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V. Quality Assurance Information

A. Quality Assurance Contacts: Richard Aburano (Manager, Reliability Engineering)
Don Lipps (Manager, Reliability Engineering)
Bryan Preeshl (Vice President of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% for all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135ºC biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 145 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 7.6 \times 10^{-9}$

λ = 7.6 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the BCD250 Process results in a FIT Rate of 1.9 @ 25ºC and 33 @ 55ºC (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot NOP0BA058D, D/C 1102)

The NP63 die type has been found to have all pins able to withstand a HBM transient pulse of +/-1500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-100mA and overvoltage per JEDEC JESD78.

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Table 1
Reliability Evaluation Test Results

MAX15012xASA+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	50 47 48	0 0 0	NOP5B1002A, D/C 0439 NOP2BA005B, D/C 0612 NOP0BA058D, D/C 1102

Note 1: Life Test Data may represent plastic DIP qualification lots.

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