RELIABILITY REPORT

FOR

MAX14979EETX+T

PLASTIC ENCAPSULATED DEVICES

October 26, 2012

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
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Quality Assurance
Reliability Engineer

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Conclusion

The MAX14979EETX+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX14979E is optimized for high-speed differential switching applications. The device is ideal for low-voltage differential signal (LVDS) and low-voltage, positive emitter-coupled logic (LVPECL) switching applications. The MAX14979E provides enhanced electrostatic discharge (ESD) protection up to ±15kV and excellent high-frequency response, making this device especially useful for interfaces that must go to an outside connection. The MAX14979E provides extremely low capacitance (CON) as well as low resistance (RON) for low-insertion loss and bandwidth up to 650MHz (1.3Gbps). In addition to the four pairs of double-pole/double-throw (DPDT) switches, the MAX14979E provides low-frequency (up to 50MHz) and AUX switching that can be used for LED lighting or other applications. The MAX14979E is available in a space-saving, 36-pin TQFN package and operates over the extended -40°C to +85°C temperature range.

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II. Manufacturing Information

A. Description/Function:	High-Bandwidth, ±15kV ESD Protection LVDS Switch
B. Process:	S4
C. Number of Device Transistors:	
D. Fabrication Location:	California, Texas or Japan
E. Assembly Location:	Taiwan, China, Thailand
F. Date of Initial Production:	April 23, 2010

III. Packaging Information

A. Package Type:	36-pin TQFN 6x6
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-2349 / A
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	38°C/W
K. Single Layer Theta Jc:	1.4°C/W
L. Multi Layer Theta Ja:	28°C/W
M. Multi Layer Theta Jc:	1.4°C/W

IV. Die Information

A. Dimensions:	61 X 100 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1 = 0.5 / Metal2 = 0.6 / Metal3 = 0.6 microns (as drawn)
F. Minimum Metal Spacing:	Metal1 = 0.45 / Metal2 = 0.5 / Metal3 = 0.6 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

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V. Quality Assurance Information

A. Quality Assurance Contacts: Richard Aburano (Manager, Reliability Engineering)
Don Lipps (Manager, Reliability Engineering)
Bryan Preeshl (Vice President of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 48 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 22.9 \times 10^{-9}$

λ = 22.9 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S4 Process results in a FIT Rate of 0.05 @ 25C and 0.83 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (Lot SX01AQ001F D/C 1025)

The AS78-1 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA and overvoltage per JEDEC JESD78.

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Table 1
Reliability Evaluation Test Results

MAX14979EETX+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	48	0	SX00AQ001D, D/C 0624

Note 1: Life Test Data may represent plastic DIP qualification lots.

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