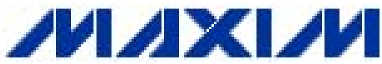

RELIABILITY REPORT

FOR

MAX14978ETO+

PLASTIC ENCAPSULATED DEVICES

August 19, 2011

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Approved by
Sokhom Chum
Quality Assurance
Reliability Engineer

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Conclusion

The MAX14978ETO+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX14978 high-performance, passive analog switch is ideal for switching Hi-Speed USB and SuperSpeed USB data between one source and two loads, or vice versa. The device can be used in desktop and notebook applications where SuperSpeed USB ports are in limited supply. The device consists of two sets of analog switches with one set used for USB low-speed, full-speed, and Hi-Speed signals and the second set used for USB SuperSpeed. The device operates from a single +3.3V supply. The device features low insertion loss for all speeds. It has ±6kV Human Body Model (HBM) ESD protection on all I/O pins. In addition, the low/full/Hi-Speed COM_ ports have ESD protection to ±15kV HBM and ±8kV IEC 61000-4-2 contact. The device is available in a small, 3.5mm × 9.0mm, 42-pin TQFN package and is specified over the extended -40°C to +85°C temperature range.

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II. Manufacturing Information

A. Description/Function:	SuperSpeed USB Passive Switch (Low/Full/Hi/SuperSpeed)	
B. Process:	TS18	S45
C. Number of Device Transistors:		
D. Fabrication Location:	Taiwan	California or Texas
E. Assembly Location:	Philippines, Thailand	
F. Date of Initial Production:	September 24, 2010	

III. Packaging Information

A. Package Type:	42-pin TQFN 3.5x9
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#31-4869 / A
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	39°C/W
K. Single Layer Theta Jc:	1.5°C/W
L. Multi Layer Theta Ja:	28°C/W
M. Multi Layer Theta Jc:	1.5°C/W

IV. Die Information

A. Dimensions:	37 X 86 mils	31 X 44 mils
B. Passivation:	SiO_2/Si_3N_4 (Silicon dioxide/ Silicon Nitride)	Si_3N_4/SiO_2 (Silicon nitride/Silicon dioxide)
C. Interconnect:	Al/Cu (0.5 %)	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None	None
E. Minimum Metal Width:	0.18 um	Metal1 = 0.5 / Metal2 = 0.6 / Metal3 = 0.6 microns (as drawn)
F. Minimum Metal Spacing:	0.18 um	Metal1 = 0.45 / Metal2 = 0.5 / Metal3 = 0.6 microns (as drawn)
G. Bondpad Dimensions:		
H. Isolation Dielectric:	SiO_2	SiO_2
I. Die Separation Method:	Wafer Saw	Wafer Saw

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V. Quality Assurance Information

A. Quality Assurance Contacts: Richard Aburano (Manager, Reliability Engineering)
Don Lipps (Manager, Reliability Engineering)
Bryan Preeshl (Vice President of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 48 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 22.9 \times 10^{-9}$

λ = 22.9 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maxim-ic.com/qa/reliability/monitor. Cumulative monitor data for the TSMC 0.18um Process results in a FIT Rate of 0.8 @ 25C and 13.1 @ 55C (0.8 eV, 60% UCL). Cumulative monitor data for the S45 Process results in a FIT Rate of 0.49 @ 25C and 8.49 @ 55C (0.8 eV, 60% UCL).

B. E.S.D. and Latch-Up Testing (lot NGGTAAA D/C 1021)

The AK14 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2000V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA and overvoltage per JEDEC JESD78.

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Table 1
Reliability Evaluation Test Results

MAX14978ETO+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	48	0	NGGTAAA, D/C 1021

Note 1: Life Test Data may represent plastic DIP qualification lots.

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