

RELIABILITY REPORT
FOR
MAX14840EATA+T
PLASTIC ENCAPSULATED DEVICES

October 22, 2013

MAXIM INTEGRATED

160 RIO ROBLES
SAN JOSE, CA 95134

Approved by
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Conclusion

The MAX14840EATA+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX14840E/MAX14841E are +3.3V ESD-protected transceivers intended for half-duplex RS-485 communication up to 40Mbps. These transceivers are optimized for high speeds over extended cable runs while maximizing tolerance to noise. The MAX14840E features symmetrical fail-safe and larger receiver hysteresis, providing improved noise rejection and improved recovered signals in high-speed and long cable applications. The MAX14841E has true fail-safe receiver inputs guaranteeing a logic-high receiver output when inputs are shorted or open. The MAX14840E/MAX14841E transceivers draw 1.5mA (typ) supply current when unloaded or when fully loaded with the drivers disabled. Hot-swap capability eliminates undesired transitions on the bus during power-up or hot insertion. The MAX14840E/MAX14841E are available in 8-pin SO and small, 8-pin (3mm x 3mm) TDFN-EP packages. Both devices operate over the -40°C to +125°C automotive temperature range.

II. Manufacturing Information

A. Description/Function:	40Mbps, +3.3V, RS-485 Half-Duplex Transceivers
B. Process:	B8
C. Number of Device Transistors:	1070
D. Fabrication Location:	California or Texas
E. Assembly Location:	Taiwan, China, Thailand, or Malaysia
F. Date of Initial Production:	January 23, 2012

III. Packaging Information

A. Package Type:	8-pin TDFN 3x3
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-3914
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	54°C/W
K. Single Layer Theta Jc:	8.3°C/W
L. Multi Layer Theta Ja:	41°C/W
M. Multi Layer Theta Jc:	8.3°C/W

IV. Die Information

A. Dimensions:	55 X 77 mils
B. Passivation:	Si ₃ N ₄ /SiO ₂ (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.8 microns (as drawn)
F. Minimum Metal Spacing:	0.8 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO ₂
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

- A. Quality Assurance Contacts: Richard Aburano (Manager, Reliability Engineering)
Don Lipps (Manager, Reliability Engineering)
Bryan Preeshl (Vice President of QA)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 48 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 22.9 \times 10^{-9}$$

$$\lambda = 22.9 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at <http://www.maximintegrated.com/qa/reliability/monitor>. Cumulative monitor data for the B8 Process results in a FIT Rate of 0.04 @ 25C and 0.73 @ 55C (0.8 eV, 60% UCL).

B. E.S.D. and Latch-Up Testing (lot JB2ZBQ001C, D/C 0941)

The RU46 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA and overvoltage per JEDEC JESD78.

Table 1
Reliability Evaluation Test Results

MAX14840EATA+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	48	0	JB2ZBQ001C, D/C 0941

Note 1: Life Test Data may represent plastic DIP qualification lots.