RELIABILITY REPORT

FOR

MAX14808ETK+T

PLASTIC ENCAPSULATED DEVICES

June 12, 2013

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
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Conclusion

The MAX14808ETK+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX14808/MAX14809 octal three-level/quad five-level, high-voltage (HV) pulser devices generate high-frequency HV bipolar pulses (up to ±105V) from low-voltage control logic inputs for driving piezoelectric transducers in ultrasound systems. All eight channels have embedded overvoltage-protection diodes and integrated active return-to-zero clamp. Both devices have embedded independent (floating) power supplies (FPS) and level shifters that allow signal transmission without the need for external HV capacitors. The MAX14808 also features eight integrated transmit/receive (T/R) switches. The MAX14809 does not have the T/R switch function. The devices feature two modes of operation: an octal three-level pulser mode (with integrated active return-to-zero clamp) or a quad five-level pulser mode. In octal three-level pulser mode, each channel is controlled by two logic inputs (DINN_/DINP_) and the active return to zero features half the current driving of the pulser 1A (typ). In quad five-level pulser mode, each channel is controlled by three logic inputs and the active return to zero has the same current driving of the pulser 2A (typ). The devices can operate both in clocked and transparent mode. In clocked mode, data inputs can be synchronized with a clean differential or single-ended clock to reduce phase noise associated with FPGA output signals that are detrimental for Doppler analysis. In transparent mode, the synchronization feature is disabled and output reflects the data input after a 18ns delay. Both devices feature adjustable maximum current (0.5A to 2A) to reduce power consumption when full current capability is not required. The devices feature integrated grass-clipping diodes (with low parasitic capacitance) for receive (Rx) and transmit (Tx) isolations. Both devices feature a damping circuit that can be activated as soon as the transmit burst is over. The damping circuit has a typical on-resistance of 500 . It fully discharges the pulser's output internal node before the grass-clipping diodes. The devices are available in a 68-pin (10mm x 10mm) TQFN package with an exposed pad and are specified over the -40°C to +85°C extended temperature range.

II. Manufacturing Information

A. Description/Function:	Octal Three-Level/Quad Five-Level High-Voltage 2A Digital Pulsers with T/R Switch
B. Process:	DM200
C. Number of Device Transistors:	11700
D. Fabrication Location:	USA
E. Assembly Location:	China, Taiwan and Thailand
F. Date of Initial Production:	September 5, 2012

III. Packaging Information

A. Package Type:	68-pin TQFN 10x10
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-4729
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 3
J. Single Layer Theta Ja:	34°C/W
K. Single Layer Theta Jc:	0.5°C/W
L. Multi Layer Theta Ja:	20°C/W
M. Multi Layer Theta Jc:	0.5°C/W

IV. Die Information

A. Dimensions:	324.8031X324.8031 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.8 microns (as drawn)
F. Minimum Metal Spacing:	2 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Richard Aburano (Manager, Reliability Engineering) Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 125°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 2454 \times 238 \times 2}$$ (Chi square value for MTTF upper limit)

(where 2454 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 8.2 \times 10^{-9}$

λ = 8.2 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the DM200 Process results in a FIT Rate of 0.33 @ 25C and 5.67 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot JAHP5Q002C, D/C 1229)

The AK19-0 die type has been found to have all pins able to withstand a HBM transient pulse of +/- 2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/- 250mA and overvoltage per JEDEC JESD78.

Table 1

Reliability Evaluation Test Results

MAX14808ETK+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 125°C	DC Parameters	79	0	JAEM3Q001C, D/C 1214
	Biased	& functionality	79	0	JAHP5Q002C, D/C 1229
	Time = 192 hrs.		80	0	JAHP63004M, D/C 1306

Note 1: Life Test Data may represent plastic DIP qualification lots.