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RELIABILITY REPORT

FOR

MAX14777GTP+T

PLASTIC ENCAPSULATED DEVICES

November 17, 2013

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
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Quality Assurance
Reliability Engineering

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Conclusion

The MAX14777GTP+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

Table of Contents

I. ....Device Description
II. ....Manufacturing Information
III. ....Packaging Information
.....Attachments
IV. ....Die Information
V. ....Quality Assurance Information
VI. ....Reliability Evaluation

I. Device Description

A. General

The MAX14777 quad SPST switch supports analog signals above and below the rails with a single 3.0V to 5.5V supply. The device features a selectable -15V/+35V or -15V/+15V analog signal range for all switches. Each switch has a separate control input to allow independent switching, making the device an alternative to opto-relays in applications that do not need galvanic isolation. The IC features 10 (max) on-resistance, and 9m (typ) RON flatness, along with a low 50nA (max at +85°C) on-leakage. For maximum signal integrity, the device keeps this performance over the entire common-mode voltage range. Each switch can carry up to 60mA (max) of continuous current in either direction. The MAX14777 is available in a 20-pin (4mm x 4mm) TQFN package and is specified over the -40°C to +105°C temperature range.

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II. Manufacturing Information

A. Description/Function:	Quad Beyond-the-Rails -15V to +35V Analog Switch
B. Process:	S18
C. Number of Device Transistors:	5440
D. Fabrication Location:	USA
E. Assembly Location:	Taiwan
F. Date of Initial Production:	June 27, 2013

III. Packaging Information

A. Package Type:	20-pin TQFN
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-5278
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	48°C/W
K. Single Layer Theta Jc:	2°C/W
L. Multi Layer Theta Ja:	33°C/W
M. Multi Layer Theta Jc:	2°C/W

IV. Die Information

A. Dimensions:	98.4252 X 92.5197 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.23 microns (as drawn)
F. Minimum Metal Spacing:	0.23 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

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V. Quality Assurance Information

A. Quality Assurance Contacts: Don Lipps (Manager, Reliability Engineering)
Bryan Preeshl (Vice President of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% for all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 157 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 7.0 \times 10^{-9}$

λ = 7.0 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S18 Process results in a FIT Rate of 0.05 @ 25°C and 0.93 @ 55°C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot EAKG7Q001C, D/C 1307)

The AK55-0 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA and overvoltage per JEDEC JESD78.

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Table 1
Reliability Evaluation Test Results

MAX14777GTP+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	157	0	EAKG7Q001, D/C 1307

Note 1: Life Test Data may represent plastic DIP qualification lots.

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