RELIABILITY REPORT

FOR

MAX14759ETA+

PLASTIC ENCAPSULATED DEVICES

January 21, 2014

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
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Quality Assurance
Reliability Engineer

Conclusion

The MAX14759ETA+ successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX14759/MAX14761/MAX14763 analog switches are capable of passing bipolar signals that are beyond their supply rails. These devices operate from a single +3.0V to +5.5V supply and support signals in the -25V to +25V range. The MAX14759 is a single-pole/single-throw (SPST) analog switch, while the MAX14761 is a dual-SPST analog switch. The MAX14763 is a single-pole/double-throw (SPDT) analog switch. The MAX14759 features 1 (max) on-resistance with a ±200nA (max) on-leakage current. The MAX14761/MAX14763 feature 2 (max) on-resistance with a ±100nA (max) on-leakage current. The low on-resistance and high bandwidth allow use in digital- and analog-signal switching applications. The MAX14759/MAX14763 are available in an 8-pin (3mm x 3mm) TDFN package. The MAX14761 is available in a 10-pin (3mm x 3mm) TDFN package. These devices are specified over the -40℃ to +85℃ extended temperature range.

II. Manufacturing Information

A. Description/Function:	Above- and Below-the-Rails Low On-Resistance Analog Switches
B. Process:	S18
C. Number of Device Transistors:	2840
D. Fabrication Location:	California
E. Assembly Location:	Taiwan, China, or Thailand
F. Date of Initial Production:	September 23, 2011

III. Packaging Information

A. Package Type:	8L TDFN
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-4301
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	1
J. Single Layer Theta Ja:	54℃/W
K. Single Layer Theta Jc:	8℃/W
L. Multi Layer Theta Ja:	41℃/W
M. Multi Layer Theta Jc:	8℃/W

IV. Die Information

A. Dimensions:	62.9921X93.7008 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.18um
F. Minimum Metal Spacing:	0.18um
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Richard Aburano (Manager, Reliability Engineering) Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% for all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 159 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 6.91 \times 10^{-9}$

$\lambda = 6.91$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S18 Process results in a FIT Rate of 0.05 @ 25C and 0.93 @ 55C (0.8 eV, 60% UCL).

B. E.S.D. and Latch-Up Testing (lot SACJ1Q002A, D/C 1147)

The AK09 die type has been found to have all pins able to withstand a transient pulse of:

ESD-HBM:	+/- 2500V per JEDEC JESD22-A114
ESD-CDM:	+/-750V per JEDEC JESD22-C101
ESD-MM:	+/-250V per JEDEC JESD22/A115

Latch-Up testing has shown that this device withstands a current of +/-100mA and overvoltage per JEDEC JESD78.

Table 1
Reliability Evaluation Test Results

MAX14759ETA+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135°C	DC Parameters	79	0	SACJ3Q002A, D/C 1149
	Biased	& functionality	80	0	SU0XBQ001A, D/C 1118
	Time = 192 hrs.				

Note 1: Life Test Data may represent plastic DIP qualification lots.