

RELIABILITY REPORT
FOR
MAX14756EUE+T
PLASTIC ENCAPSULATED DEVICES

October 15, 2012

MAXIM INTEGRATED

160 RIO ROBLES
SAN JOSE, CA 95134

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Conclusion

The MAX14756EUE+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX14756/MAX14757/MAX14758 are analog switches with a low on-resistance of 10 Ω (max) that conduct equally well in both directions. All devices have a rail-to-rail analog-signal range. They operate with a single +10V to +70V supply in unipolar applications with ± 35 V dual supplies in bipolar applications. The bipolar supplies can be offset and do not have to be symmetrical. The MAX14756 is a quad normally closed (NC) single-pole/single-throw (SPST) switch, the MAX14757 is a quad normally open (NO) SPST switch, and the MAX14758 has two NO and two NC SPST switches. These switches have 5 Ω (typ) on-resistances and low on-leakage currents of 0.01nA (typ). The on-resistance flatness is 0.004 (typ). The devices are suitable for a multitude of analog signal routing and switching applications. They are specified over an extended temperature range of -40°C to +85°C, but can be operated up to +125°C with elevated leakage currents.

II. Manufacturing Information

A. Description/Function:	Quad SPST +70V Analog Switches
B. Process:	BCD88
C. Number of Device Transistors:	3899
D. Fabrication Location:	USA
E. Assembly Location:	Malaysia, Philippines and Thailand
F. Date of Initial Production:	December 22, 2010

III. Packaging Information

A. Package Type:	16-pin TSSOP
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-4142
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	106°C/W
K. Single Layer Theta Jc:	27°C/W
L. Multi Layer Theta Ja:	90°C/W
M. Multi Layer Theta Jc:	27°C/W

IV. Die Information

A. Dimensions:	83 X 134 mils
B. Passivation:	Si ₃ N ₄ /SiO ₂ (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1 = 1.0 / Metal2 = 3.0 microns (as drawn)
F. Minimum Metal Spacing:	Metal1 = 2.0 / Metal2 = 3.0 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO ₂
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

- A. Quality Assurance Contacts: Richard Aburano (Manager, Reliability Engineering)
Don Lipps (Manager, Reliability Engineering)
Bryan Preeshl (Vice President of QA)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 48 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 22.9 \times 10^{-9}$$

$$\lambda = 22.9 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at <http://www.maximintegrated.com/qa/reliability/monitor>. Cumulative monitor data for the BCD88 Process results in a FIT Rate of 0.36 @ 25C and 6.17 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot JJ5ZCQ001G, D/C 1134)

The AK11 die type has been found to have all pins able to withstand a HBM transient pulse of +/- 2000V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/- 100mA and overvoltage per JEDEC JESD78.

Table 1
Reliability Evaluation Test Results

MAX14756EUE+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	48	0	JJ5XBQ001D, D/C 1040

Note 1: Life Test Data may represent plastic DIP qualification lots.