

RELIABILITY REPORT  
FOR  
MAX14724ETP+T  
PLASTIC ENCAPSULATED DEVICES

September 22, 2016

**MAXIM INTEGRATED**

160 RIO ROBLES  
SAN JOSE, CA 95134

<b>Approved by</b>
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Quality Assurance
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## Conclusion

The MAX14724ETP+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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### I. Device Description

#### A. General

The MAX14724 is a serial-controlled, 8:4 full-matrix analog multiplexer. The device operates from either a single wide supply or dual  $\pm 2.5V$  supplies. A wide operating range makes the device ideal for battery-powered, portable instruments. All channels guarantee break-before-make switching. The serial control is selectable between I<sup>2</sup>C and SPI. Both modes provide individual control of each independent switch so that any combination of switches can be applied. I<sup>2</sup>C mode provides one address-select pin, allowing for addressing up to two devices on a single bus. The SPI mode includes a DO pin that can be used to daisy-chain multiple devices together with a single select signal. The MAX14724 features bidirectional operation and can handle rail-to-rail analog signals. All control inputs are 1.6V-logic compatible. This device is available in a small 20-pin, 4mm × 4mm, TQFN and 20-bump, 2mm × 1.7mm, wafer-level package (WLP).

## II. Manufacturing Information

A. Description/Function:	Serial-Controlled 8:4 Matrix Switch Multiplexer
B. Process:	S18
C. Number of Device Transistors:	20068
D. Fabrication Location:	USA
E. Assembly Location:	Taiwan
F. Date of Initial Production:	June 24, 2016

## III. Packaging Information

A. Package Type:	20-pin TQFN
B. Lead Frame:	Copper
C. Lead Finish:	100% Matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Cu (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-5852
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	59°C/W
K. Single Layer Theta Jc:	6°C/W
L. Multi Layer Theta Ja:	39°C/W
M. Multi Layer Theta Jc:	6°C/W

## IV. Die Information

A. Dimensions:	81.1023X65.3543 mils
B. Passivation:	Si <sub>3</sub> N <sub>4</sub> /SiO <sub>2</sub> (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.23 microns (as drawn)
F. Minimum Metal Spacing:	0.23 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO <sub>2</sub>
I. Die Separation Method:	Wafer Saw

## V. Quality Assurance Information

- A. Quality Assurance Contacts: Eric Wright (Reliability Engineering)  
Bryan Preeshl (Vice President of QA)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.  
0.1% for all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

## VI. Reliability Evaluation

### A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate ( $\lambda$ ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 80 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 13.7 \times 10^{-9}$$

$$\lambda = 13.7 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at <http://www.maximintegrated.com/qa/reliability/monitor>. Cumulative monitor data for the S18 Process results in a FIT Rate of 0.40 @ 25C and 6.96 @ 55C (0.8 eV, 60% UCL)

### B. E.S.D. and Latch-Up Testing

The MAX14724 has been found to have all pins able to withstand a transient pulse of:

ESD-HBM: +/- 2500V per JEDEC JESD22-A114

ESD-CDM: +/- 750V per JEDEC JESD22-C101

Latch-Up testing has shown that this device withstands a current of +/-250mA and overvoltage per JEDEC JESD78

**Table 1**  
Reliability Evaluation Test Results

**MAX14724ETP+T**

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
<b>Static Life Test</b> (Note 1)	Ta = 135C Biased Time = 192 hrs.	DC Parameters & functionality	80	0	

Note 1: Life Test Data may represent plastic DIP qualification lots.