RELIABILITY REPORT

FOR

MAX14691ATP+T

PLASTIC ENCAPSULATED DEVICES

May 14, 2015

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
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Quality Assurance
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Conclusion

The MAX14691ATP+T successfully met the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX14691-MAX14693 adjustable overvoltage, undervoltage, and overcurrent protection devices guard systems against overcurrent faults in addition to positive overvoltage and reverse-voltage faults. When used with an optional external p-channel MOSFET, the devices also protect downstream circuitry from voltage faults up to ±60V. The devices feature a low, 31mÎ©, on-resistance integrated FET.

During startup, the devices are designed to charge large capacitances on the output in a continuous mode for applications where large reservoir capacitors are used on the inputs to downstream devices.

Additionally, the devices feature a dual-stage, current-limit mode in which the current is continuously limited to 1x, 1.5x, and 2x the programmed limit, respectively, for a short time after startup. This enables faster charging of large loads during startup.

The MAX14691-MAX14693 also features reverse-current and overtemperature protection. The devices are available in a 20-pin (5mm x 5mm) TQFN package and operate over the -40°C to 125°C temperature range.

II. Manufacturing Information

A. Description/Function:	High-Accuracy, Adjustable Power Limiter
B. Process:	S18
C. Number of Device Transistors:	22569
D. Fabrication Location:	Japan
E. Assembly Location:	Taiwan
F. Date of Initial Production:	June 26, 2014

III. Packaging Information

A. Package Type:	20-pin TQFN
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Cu (2 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-5567
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	47°C/W
K. Single Layer Theta Jc:	2°C/W
L. Multi Layer Theta Ja:	29°C/W
M. Multi Layer Theta Jc:	2°C/W

IV. Die Information

A. Dimensions:	106.2992 X 139.7637 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.23 microns (as drawn)
F. Minimum Metal Spacing:	0.23 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% for all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 79 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 13.9 \times 10^{-9}$

$\lambda = 13.9$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S18 Process results in a FIT Rate of 0.05 @ 25°C and 0.93 @ 55°C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing

The AL72-0 die type has been found to have all pins able to withstand an HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-100mA and overvoltage per JEDEC JESD78.

Table 1

Reliability Evaluation Test Results

MAX14691ATP+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	79	0	

Note 1: Life Test Data may represent plastic DIP qualification lots.