RELIABILITY REPORT

FOR

MAX14670EWL+T

WAFER LEVEL PRODUCTS

June 3, 2013

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
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Quality Assurance
Manager, Reliability Engineering

Conclusion

The MAX14670EWL+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX14670–MAX14673 provides protection to valuable consumer circuits against positive voltage faults up to +28VDC. An internal clamp also protects the devices from surges up to +100V. The device is able to disconnect the system from its output terminal when wrong input conditions are detected. The MAX14670–MAX14673 overvoltage protection devices feature low 70mΩ (typ), WLP package on-resistance (RON) internal FETs, effectively minimizing a voltage drop across the device. When the input voltage exceeds the overvoltage threshold, the internal FET is turned off to prevent damage to the protected components. The overvoltage protection threshold can be adjusted with optional external resistors to any voltage between 5V and 22V. The devices automatically choose the accurate internal trip thresholds when the overvoltage lockout input (OVLO) is set lower than the external OVLO select voltage. The internal OVLO are preset to typical 6.8V (MAX14670), 15.5V (MAX14671), 5.825V (MAX14672), or 22V (MAX14673). The MAX14670–MAX14673 feature reverse bias blocking capability. Unlike other overvoltage protectors, when the MAX14670-MAX14673 are disabled, the voltage applied to OUT does not feed back into IN. These devices also feature an OTG enable pin that allows OUT voltage to supply IN. The MAX14670-MAX14673 also have thermal shutdown protection against over load condition. The MAX14670-MAX14673 are specified over the extended -40°C to +85°C temperature range. The MAX14670/MAX14671 are available in a 15-bump WLP package and the MAX14672/MAX14673 are available in a 10-pin TDFN package.

II. Manufacturing Information

A. Description/Function:	Bidirectional High-Input Overvoltage Protector with Adjustable OVLO
B. Process:	S18
C. Number of Device Transistors:	3297
D. Fabrication Location:	Japan
E. Assembly Location:	USA
F. Date of Initial Production:	2013

III. Packaging Information

A. Package Type:	15-ball WLP 3x5 array
B. Lead Frame:	N/A
C. Lead Finish:	N/A
D. Die Attach:	None
E. Bondwire:	N/A (N/A mil dia.)
F. Mold Material:	None
G. Assembly Diagram:	#05-9000-5237
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	°C/W
K. Single Layer Theta Jc:	°C/W
L. Multi Layer Theta Ja:	52°C/W
M. Multi Layer Theta Jc:	°C/W

IV. Die Information

A. Dimensions:	62.9921X85.4331 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.23 microns (as drawn)
F. Minimum Metal Spacing:	0.23 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Richard Aburano (Manager, Reliability Engineering) Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 162 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 6.8 \times 10^{-9}$

$\lambda = 6.8$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S18 Process results in a FIT Rate of 0.05 @ 25C and 0.93 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot EAMA5Q003E, D/C 1313)

The AL60-0 die type has been found to have all pins able to withstand a HBM transient pulse of +/- 2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/- 250mA and overvoltage per JEDEC JESD78.

Table 1
Reliability Evaluation Test Results

MAX14670EWL+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	162	0	EAMA5Q003E, D/C 1313

Note 1: Life Test Data may represent plastic DIP qualification lots.