RELIABILITY REPORT

FOR

MAX14655EWC+T

WAFER LEVEL PRODUCTS

March 19, 2013

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
Sokhom Chum
Quality Assurance
Reliability Engineer

Conclusion

The MAX14655EWC+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX14653/MAX14654/MAX14655 overvoltage protection devices feature a low 38m (typ) RON internal FET and protect low-voltage systems against voltage faults up to +28VDC. An internal clamp also protects the devices from surges up to +80V. When the input voltage exceeds the overvoltage threshold, the internal FET is turned off to prevent damage to the protected downstream components. The overvoltage protection threshold can be adjusted with optional external resistors to any voltage between 4V and 20V. With the OVLO input set below the external OVLO select voltage, the MAX14653/MAX14654/MAX14655 automatically choose the accurate internal trip thresholds. The internal overvoltage thresholds (OVLO) are preset to 15.5V typical (MAX14653), 6.8V typical (MAX14654), or 5.825V typical (MAX14655). The devices feature an open-drain active-low ACOK output indicating a stable supply between minimum supply voltage and VOVLO. The MAX14653/MAX14654/MAX14655 are also protected against overcurrent events by an internal thermal shutdown. The MAX14653/MAX14654/MAX14655 are offered in a small 12-bump WLP package and operate over the -40°C to +85°C extended temperature range.

II. Manufacturing Information

A. Description/Function:	High-Current Overvoltage Protector with Integrated Surge Protection
B. Process:	S18
C. Number of Device Transistors:	2971
D. Fabrication Location:	California
E. Assembly Location:	Texas
F. Date of Initial Production:	December 20, 2012

III. Packaging Information

A. Package Type:	3x4 12 bmp WLP
B. Lead Frame:	N/A
C. Lead Finish:	N/A
D. Die Attach:	N/A
E. Bondwire:	N/A
F. Mold Material:	
G. Assembly Diagram:	#05-9000-5163
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	1
J. Single Layer Theta Ja:	N/A
K. Single Layer Theta Jc:	N/A
L. Multi Layer Theta Ja:	73°C/W
M. Multi Layer Theta Jc:	N/A

IV. Die Information

A. Dimensions:	51.9685X73.2283 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.18um
F. Minimum Metal Spacing:	0.18um
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Richard Aburano (Manager, Reliability Engineering) Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135¿C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 79 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 13.9 \times 10^{-9}$

$\lambda = 13.9$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S18 Process results in a FIT Rate of 0.05 @ 25C and 0.93 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot EAJA0Q001A D/C 1240)

The AL57-0 die type has been found to have all pins able to withstand a transient pulse of:

ESD-HBM:	+/- 2500V per JEDEC JESD22-A114
ESD-CDM:	+/- 750V per JEDEC JESD22-C101

Latch-Up testing has shown that this device withstands a current of+/- 250mA and overvoltage per JEDEC JESD78.

Table 1

Reliability Evaluation Test Results

MAX14655EWC+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	79	0	EAJA0Q001A, D/C 1240

Note 1: Life Test Data may represent plastic DIP qualification lots.