



RELIABILITY REPORT  
FOR  
MAX14607EWL+T  
WAFER LEVEL PRODUCTS

February 17, 2012

**MAXIM INTEGRATED PRODUCTS**

120 SAN GABRIEL DR.  
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## Conclusion

The MAX14607EWL+T successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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### I. Device Description

#### A. General

The MAX14606/MAX14607 overvoltage protection devices feature low 54m (typ) on-resistance (RON) internal FETs and protect low-voltage systems against voltage faults up to +36V. When the input voltage exceeds the overvoltage threshold, the internal FET is turned off to prevent damage to the protected components. The devices automatically choose the accurate internal trip thresholds. The internal OVLO are preset to typical 5.87V (MAX14606) or 6.8V (MAX14607). The MAX14606/MAX14607 feature reverse bias blocking capability. Unlike other overvoltage protectors, when the MAX14606/MAX14607 are disabled, the voltage applied to OUT does not feed back into IN. These devices also feature thermal shutdown to protect against overcurrent events. The MAX14606/MAX14607 are specified over the extended -40°C to +85°C temperature range, and are available in 9-bump WLP packages.

## II. Manufacturing Information

A. Description/Function:	Overvoltage Protectors with Reverse Bias Blocking
B. Process:	S18
C. Number of Device Transistors:	1877
D. Fabrication Location:	USA
E. Assembly Location:	Japan and USA
F. Date of Initial Production:	December 21, 2011

## III. Packaging Information

A. Package Type:	9-bump WLP 3x3 array
B. Lead Frame:	N/A
C. Lead Finish:	N/A
D. Die Attach:	None
E. Bondwire:	N/A (N/A mil dia.)
F. Mold Material:	None
G. Assembly Diagram:	#05-9000-4622
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	°C/W
K. Single Layer Theta Jc:	°C/W
L. Multi Layer Theta Ja:	84°C/W
M. Multi Layer Theta Jc:	°C/W

## IV. Die Information

A. Dimensions:	51.97X51.97 mils
B. Passivation:	Si <sub>3</sub> N <sub>4</sub> /SiO <sub>2</sub> (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1 = 0.23 / Metal2-3 = 0.28 / Metal 4 = 2.6 microns (as drawn)
F. Minimum Metal Spacing:	Metal1 = 0.23 / Metal2-3 = 0.28 / Metal 4 = 3.0 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO <sub>2</sub>
I. Die Separation Method:	Wafer Saw

## V. Quality Assurance Information

- A. Quality Assurance Contacts: Richard Aburano (Manager, Reliability Engineering)  
Don Lipps (Manager, Reliability Engineering)  
Bryan Preeshl (Vice President of QA)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.  
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

## VI. Reliability Evaluation

### A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate ( $\lambda$ ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 80 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 13.7 \times 10^{-9}$$

$$\lambda = 13.7 \text{ F.I.T. (60\% confidence level @ 25}^\circ\text{C)}$$

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at <http://www.maxim-ic.com/qa/reliability/monitor>. Cumulative monitor data for the Process results in a FIT Rate of 0.06 @ 25C and 1.04 @ 55C (0.8 eV, 60% UCL)

### B. E.S.D. and Latch-Up Testing (lot SABX7Q001B, D/C 1143)

The AL36-1 die type has been found to have all pins able to withstand a HBM transient pulse of +/- 2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/- 100mA and overvoltage per JEDEC JESD78.

**Table 1**  
Reliability Evaluation Test Results

**MAX14607EWL+T**

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
<b>Static Life Test</b> (Note 1)	Ta = 135C Biased Time = 192 hrs.	DC Parameters & functionality	80	0	SABX6Q001A, D/C 1142

Note 1: Life Test Data may represent plastic DIP qualification lots.