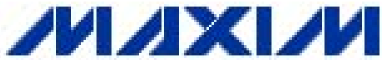

RELIABILITY REPORT

FOR

MAX14590ETA+T

PLASTIC ENCAPSULATED DEVICES

August 14, 2012

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Approved by
Richard Aburano
Quality Assurance
Manager, Reliability Engineering

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Conclusion

The MAX14590ETA+T successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX14586/MAX14590 overvoltage protection devices feature a low 48mΩ (typ) on-resistance (RON) internal FET and protect low-voltage systems against voltage faults up to +36V. When the input voltage exceeds the overvoltage threshold, the internal FET is turned off to prevent damage to the protected components. The overvoltage protection threshold can be adjusted with optional external resistors to any voltage between 4V and 20V. With the OVLO input set below the external OVLO select voltage, the devices automatically choose the internal accurate trip thresholds. The internal overvoltage thresholds (OVLO) are preset to 7V typical (MAX14586) or 15V typical (MAX14590). The devices are also protected against overcurrent events by an internal thermal shutdown. The MAX14586/MAX14590 are offered in a small, 8-pin TDFN package with exposed pad and operate over the -40°C to +85°C extended temperature range.

II. Manufacturing Information

A. Description/Function:	High-Current Overvoltage Protectors with Adjustable OVLO
B. Process:	S18
C. Number of Device Transistors:	1745
D. Fabrication Location:	USA
E. Assembly Location:	China, Taiwan and Thailand
F. Date of Initial Production:	March 25, 2011

III. Packaging Information

A. Package Type:	8-pin TDFN 2x2
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-4429
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	110°C/W
K. Single Layer Theta Jc:	37°C/W
L. Multi Layer Theta Ja:	83.9°C/W
M. Multi Layer Theta Jc:	37°C/W

IV. Die Information

A. Dimensions:	34.65X63.78 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1 = 0.23 / Metal2-3 = 0.28 / Metal 4 = 2.6 microns (as drawn)
F. Minimum Metal Spacing:	Metal1 = 0.23 / Metal2-3 = 0.28 / Metal 4 = 3.0 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

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V. Quality Assurance Information

A. Quality Assurance Contacts: Richard Aburano (Manager, Reliability Engineering)
Don Lipps (Manager, Reliability Engineering)
Bryan Preeshl (Vice President of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 77 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 14.3 \times 10^{-9}$

λ = 14.3 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maxim-ic.com/qa/reliability/monitor. Cumulative monitor data for the S18 Process results in a FIT Rate of 0.03 @ 25C and 0.58 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot SZ9YAQ001C, D/C 1112)

The AL29-1 die type has been found to have all pins able to withstand a HBM transient pulse of +/- 2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/- 250mA and overvoltage per JEDEC JESD78.

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Table 1

Reliability Evaluation Test Results

MAX14590ETA+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135C Biased Time = 192 hrs.	DC Parameters & functionality	77	0	SZ9ZAQ001C, D/C 1109

Note 1: Life Test Data may represent plastic DIP qualification lots.

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