RELIABILITY REPORT

FOR

MAX14589EEWL+T

WAFER LEVEL PRODUCTS

November 12, 2012

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
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Quality Assurance
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Conclusion

The MAX14589EEWL+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX14589E/MAX14594E high-density, double-pole/double-throw (DPDT) analog switches feature Beyond-the-Rails(tm) signal capability that allows signals from -5.5V to +5.5V to pass without distortion even when the power supply is below the signal range. The low RON resistance (0.2) makes the devices ideal for low-distortion switching, such as audio. The MAX14594E has internal shunt switches that discharge the audio amplifier AC-coupling capacitance at the normally open (NO1 and NO2) terminals. This feature reduces click-and-pop sounds that occur when switching audio signals between precharged points. The switches are fully specified to operate from a single +1.6V to +5.5V power supply. Because of the low supply current requirement, VCCEN can be provided by a GPIO. When the power is not applied, switches go to a high-impedance mode and all analog signal ports can withstand signals from -5.5V to +5.5V. The devices control the switches with a control bit, CB. The MAX14589E/MAX14594E are available in a 1.2mm × 1.2mm, 0.4mm pitch, 9-bump wafer-level package (WLP) and operate over the -40°C to +85°C extended temperature range.

II. Manufacturing Information

A. Description/Function:	High-Density, ±5V Capable DPDT Analog Switches
B. Process:	S18
C. Number of Device Transistors:	1626
D. Fabrication Location:	USA
E. Assembly Location:	Japan and USA
F. Date of Initial Production:	June 28, 2012

III. Packaging Information

A. Package Type:	9-bump WLP 3x3 array
B. Lead Frame:	N/A
C. Lead Finish:	N/A
D. Die Attach:	None
E. Bondwire:	N/A (N/A mil dia.)
F. Mold Material:	None
G. Assembly Diagram:	#05-9000-4480
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	°C/W
K. Single Layer Theta Jc:	°C/W
L. Multi Layer Theta Ja:	83°C/W
M. Multi Layer Theta Jc:	°C/W

IV. Die Information

A. Dimensions:	50X50 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1 = 0.23 / Metal2-3 = 0.28 / Metal 4 = 2.6 microns (as drawn)
F. Minimum Metal Spacing:	Metal1 = 0.23 / Metal2-3 = 0.28 / Metal 4 = 3.0 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Richard Aburano (Manager, Reliability Engineering) Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 80 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 13.7 \times 10^{-9}$

λ = 13.7 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S18 Process results in a FIT Rate of 0.06 @ 25C and 1.05 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot SAGG5Q003D, D/C 1217)

The AL27 die type has been found to have all pins able to withstand a HBM transient pulse of +/- 2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/- 250mA and overvoltage per JEDEC JESD78.

Table 1

Reliability Evaluation Test Results

MAX14589EEWL+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	80	0	SAGG5Q003D, D/C 1217

Note 1: Life Test Data may represent plastic DIP qualification lots.