RELIABILITY REPORT

FOR

MAX14585AEVB+T

PLASTIC ENCAPSULATED DEVICES

November 10, 2017

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

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Conclusion

The MAX14585AEVB+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX14585/MAX14585A high-ESD-protected double-pole/double-throw (DPDT) switches multiplex Hi-Speed (480Mbps) USB and analog signals such as AC-coupled audio or video. These devices combine the low on-capacitance (CON) and low on-resistance (RON) necessary for high-performance switching applications in portable electronics and include an internal negative supply to pass audio signals that swing below ground down to -1.8V. The devices also handle USB low-/full-speed signaling and operate from a 2.7V to 5.5V supply. The devices feature a VBUS detection input (VB) that can handle voltage up to 28V to automatically switch to the USB signal path upon detection of a valid VBUS signal (VB > VVBDET). In a dead battery situation, the voltage on VB can supply power to the part if VB is greater than 4.5V. The MAX14585 features internal shunt resistors on the audio path to reduce clicks and pops heard at the output. The MAX14585/MAX14585A are available in a space-saving, 10-pin, 1.4mm x 1.8mm UTQFN package and operate over the -40°C to +85°C temperature range.

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II. Manufacturing Information

A. Description/Function:	Hi-Speed USB and Audio Switches with Negative Signal Capability and High-Voltage-Tolerant V_{BUS} Detection
B. Process:	S18
C. Number of Device Transistors:	1898
D. Fabrication Location:	USA
E. Assembly Location:	Taiwan, Thailand
F. Date of Initial Production:	March 25, 2011

III. Packaging Information

A. Package Type:	10-pin UTQFN
B. Lead Frame:	Copper
C. Lead Finish:	NiPdAu
D. Bondwire:	Au (1 mil dia.)
E. Mold Material:	Epoxy with silica filler
F. Assembly Diagram:	#05-9000-4366
G. Flammability Rating:	Class UL94-V0
H. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
I. Single Layer Theta Ja:	N/A°C/W
J. Single Layer Theta Jc:	N/A°C/W
K. Multi Layer Theta Ja:	143.2°C/W
L. Multi Layer Theta Jc:	20.1°C/W

IV. Die Information

A. Dimensions:	29.5276X37.4016 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.23 microns (as drawn)
F. Minimum Metal Spacing:	0.23 microns (as drawn)
G. Isolation Dielectric:	SiO_2
H. Die Separation Method:	Wafer Saw

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V. Quality Assurance Information

A. Quality Assurance Contacts: Eric Wright (Reliability Engineering)
Brian Standley (Manager, Reliability)
Bryan Preeshl (Vice President of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% for all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 48 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 22.9 \times 10^{-9}$

λ = 22.9 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S18 Process results in a FIT Rate of 0.40 @ 25C and 6.96 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing

The AL20-1 die type has been found to have all pins able to withstand an HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA and overvoltage per JEDEC JESD78.

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Table 1
Reliability Evaluation Test Results

MAX14585AEVB+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135C Biased Time = 192 hrs.	DC Parameters & functionality	48	0	

Note 1: Life Test Data may represent plastic DIP qualification lots.

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