RELIABILITY REPORT

FOR

MAX14581EWC+T

WAFER LEVEL PRODUCTS

October 21, 2012

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
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Conclusion

The MAX14581EWC+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX14581/MAX14582 USB-compliant transceivers are designed to minimize the area and external components required to interface low-voltage ASICs to USB. These devices comply with USB 2.0 specification for fullspeed-only (12Mbps) operation. The transceivers include an internal 3.3V regulator, an internal 1.5k D+ pullup resistor, and built-in ±15kV ESD HBM protection circuitry to protect the USB I/O ports (D+, D-). The MAX14581/MAX14582 also have internal series resistors, allowing the devices to be wired directly to a USB connector. These devices operate with logic-supply voltages as low as +1.2V, ensuring compatibility with low-voltage ASICs. A low-power disable mode reduces current consumption to typically less than 13µA (typ) from VBUS. An enumerate function controls the D+ pullup resistor, allowing devices to logically disconnect while remaining plugged in. The devices have 36 (typ) internal series resistors on D+/D- for direct connection to the USB connector. These devices can be used as either peripheral or host (FS) USB transceivers. As a host USB transceiver, the MAX14581/MAX14582 require external 15k pulldown resistors and driving ENUM logic-low. The MAX14581 (3-wire) is equipped with DAT and SE0 interface signals. The transceiver provides a USB detection function that monitors the presence of USB VBUS and signals the event by means of a BD pin. The MAX14582 (5-wire) is equipped with VP, VM, and RCV interface signals. The detection of VBUS in the MAX14582 is encoded as VP = VM = logic-high. These devices operate over the extended -40°C to +85°C temperature range and are available in 12-bump WLP packages.

II. Manufacturing Information

A. Description/Function:	Industry's Smallest and Lowest (V_L) Full-Speed USB Transceivers, with Low VIO 3/5-Wire Interface
B. Process:	S18
C. Number of Device Transistors:	5374
D. Fabrication Location:	California
E. Assembly Location:	Japan and USA
F. Date of Initial Production:	June 28, 2012

III. Packaging Information

A. Package Type:	12-bump WLP 3x4 array
B. Lead Frame:	N/A
C. Lead Finish:	N/A
D. Die Attach:	None
E. Bondwire:	N/A (N/A mil dia.)
F. Mold Material:	None
G. Assembly Diagram:	#05-9000-4690
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	°C/W
K. Single Layer Theta Jc:	°C/W
L. Multi Layer Theta Ja:	73°C/W
M. Multi Layer Theta Jc:	°C/W

IV. Die Information

A. Dimensions:	65.3543X50 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1 = 0.23 / Metal2-3 = 0.28 / Metal 4 = 2.6 microns (as drawn)
F. Minimum Metal Spacing:	Metal1 = 0.23 / Metal2-3 = 0.28 / Metal 4 = 3.0 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

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V. Quality Assurance Information

A. Quality Assurance Contacts: Richard Aburano (Manager, Reliability Engineering)
Don Lipps (Manager, Reliability Engineering)
Bryan Preeshl (Vice President of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 80 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 13.7 \times 10^{-9}$

λ = 13.7 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S18 Process results in a FIT Rate of 0.06 @ 25C and 1.04 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot SAFF7Q001B, D/C 1212)

The AL34-0 die type has been found to have all pins able to withstand a HBM transient pulse of +/- 1500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/- 250mA and overvoltage per JEDEC JESD78.

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Table 1
Reliability Evaluation Test Results

MAX14581EWC+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	80	0	SAFF7Q001B, D/C 1212

Note 1: Life Test Data may represent plastic DIP qualification lots.

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