

RELIABILITY REPORT
FOR
MAX14573EUD+T
PLASTIC ENCAPSULATED DEVICES

March 18, 2013

MAXIM INTEGRATED

160 RIO ROBLES
SAN JOSE, CA 95134

Approved by
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Conclusion

The MAX14573EUD+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

Table of Contents

I.Device Description	IV.Die Information
II.Manufacturing Information	V.Quality Assurance Information
III.Packaging Information	VI.Reliability Evaluation
.....Attachments	

I. Device Description

A. General

The MAX14571/MAX14572/MAX14573 adjustable overvoltage-and overcurrent-protection devices are ideal to protect systems against positive and negative input voltage faults up to $\pm 40V$ and feature low 100m (typ) RON FETs. The overvoltage-protector (OVP) feature protects voltages between 6V and 36V, while the undervoltage-protector (UVP) feature protects voltages between 4.5V and 24V. The overvoltage-lockout (OVLO) and undervoltage-lockout (UVLO) thresholds are set using optional external resistors. The factory-preset internal OVLO threshold is 33V (typ) and the preset internal UVLO threshold is 19.2V (typ). The ICs also feature programmable current-limit protection up to 4.2A. Once current reaches the threshold, the MAX14571 turns off after the 20.7ms (typ) blanking time and stays off during the retry period. The MAX14572 latches off after the blanking time, and the MAX14573 limits the current continuously. In addition, these devices feature reverse current and thermal-shutdown protection. The ICs are available in a small 14-pin TSSOP (5mm x 6.5mm) package and are specified over the extended -40°C to +85°C temperature range.

II. Manufacturing Information

A. Description/Function:	Adjustable Overvoltage and Overcurrent Protectors with High Accuracy
B. Process:	S18
C. Number of Device Transistors:	4721
D. Fabrication Location:	USA
E. Assembly Location:	Thailand and Philippines
F. Date of Initial Production:	December 20, 2012

III. Packaging Information

A. Package Type:	14-pin TSSOP
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-4951
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	48°C/W
K. Single Layer Theta Jc:	3°C/W
L. Multi Layer Theta Ja:	39°C/W
M. Multi Layer Theta Jc:	3°C/W

IV. Die Information

A. Dimensions:	103.5433X83.4645 mils
B. Passivation:	Si ₃ N ₄ /SiO ₂ (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.23 microns (as drawn)
F. Minimum Metal Spacing:	0.23 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO ₂
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

- A. Quality Assurance Contacts: Richard Aburano (Manager, Reliability Engineering)
Don Lipps (Manager, Reliability Engineering)
Bryan Preeshl (Vice President of QA)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 159 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 6.9 \times 10^{-9}$$

$$\lambda = 6.9 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at <http://www.maximintegrated.com/qa/reliability/monitor>. Cumulative monitor data for the S18 Process results in a FIT Rate of 0.05 @ 25C and 0.93 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot SAJO1Q002A, D/C 1243)

The AL08-2 die type has been found to have all pins able to withstand a HBM transient pulse of +/- 2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/- 100mA per JEDEC JESD78 and up to an overvoltage limit of 48V which is beyond AMR.

Table 1
Reliability Evaluation Test Results

MAX14573EUD+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135°C	DC Parameters	79	0	SAIE9Q001C, D/C 1229
	Biased	& functionality	80	0	SAIE9Q001D, D/C 1229
	Time = 192 hrs.				

Note 1: Life Test Data may represent plastic DIP qualification lots.