

RELIABILITY REPORT
FOR
MAX1452ATG+
PLASTIC ENCAPSULATED DEVICES

April 20, 2012

MAXIM INTEGRATED PRODUCTS

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Approved by
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Conclusion

The MAX1452ATG+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX1452 is a highly integrated analog-sensor signal processor optimized for industrial and process control applications utilizing resistive element sensors. The MAX1452 provides amplification, calibration, and temperature compensation that enables an overall performance approaching the inherent repeatability of the sensor. The fully analog signal path introduces no quantization noise in the output signal while enabling digitally controlled trimming with the integrated 16-bit DACs. Offset and span are calibrated using 16-bit DACs, allowing sensor products to be truly interchangeable. The MAX1452 architecture includes a programmable sensor excitation, a 16-step programmable-gain amplifier (PGA), a 768-byte (6144 bits) internal EEPROM, four 16-bit DACs, an uncommitted op amp, and an on-chip temperature sensor. In addition to offset and span compensation, the MAX1452 provides a unique temperature compensation strategy for offset TC and FSOTC that was developed to provide a remarkable degree of flexibility while minimizing testing costs. The MAX1452 is packaged for the commercial, industrial, and automotive temperature ranges in 16-pin SSOP/TSSOP and 24-pin TQFN packages.

II. Manufacturing Information

A. Description/Function:	Low-Cost Precision Sensor Signal Conditioner
B. Process:	TS50
C. Number of Device Transistors:	
D. Fabrication Location:	Taiwan
E. Assembly Location:	China
F. Date of Initial Production:	Pre 1997

III. Packaging Information

A. Package Type:	24L TQFN
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-1082 / B
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	1
J. Single Layer Theta Ja:	48°C/W
K. Single Layer Theta Jc:	3°C/W
L. Multi Layer Theta Ja:	36°C/W
M. Multi Layer Theta Jc:	3°C/W

IV. Die Information

A. Dimensions:	91 X 88 mils
B. Passivation:	Si ₃ N ₄ /SiO ₂ (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.50µm
F. Minimum Metal Spacing:	0.50µm
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO ₂
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

- A. Quality Assurance Contacts: Richard Aburano (Manager, Reliability Engineering)
Don Lipps (Manager, Reliability Engineering)
Bryan Preeshl (Vice President of QA)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{1000 \times 4340 \times 80 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 2.6 \times 10^{-9}$$

$$\lambda = 2.6 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at <http://www.maxim-ic.com/qa/reliability/monitor>. Cumulative monitor data for the TS50 Process results in a FIT Rate of 0.25 @ 25C and 6.11 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (ESD lot K91ABA008A D/C 0414, Latch-Up lot K91AEA035A D/C 0523)

The SC02 die type has been found to have all pins able to withstand a HBM transient pulse of:

- ESD-HBM: +/- 1000V per JEDEC JESD22-A114
- ESD-CDM: +/- 500V per JEDEC JESD22-C101

Latch-Up testing has shown that this device withstands a current of +/- 250mA.

Table 1
Reliability Evaluation Test Results

MAX1452ATG+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135°C Biased Time = 1000 hrs.	DC Parameters & functionality	80	0	K91ABA008A, D/C 0414

Note 1: Life Test Data may represent plastic DIP qualification lots.