

RELIABILITY REPORT
FOR
MAX14436FAWE+T

PLASTIC ENCAPSULATED DEVICES

January 3, 2018

# **MAXIM INTEGRATED**

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#### Conclusion

The MAX14436FAWE+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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#### I. Device Description

#### A. General

The MAX14434—MAX14436 are the fastest, lowest power, 4-channel, digital galvanic isolators on the market today using Maxim's proprietary process technology. These devices transfer digital signals between circuits with different power domains while using as little as 0.58mW per channel at 1Mbps with a 1.8V supply. The MAX14434/5/6 have an isolation rating of 5kV<sub>RMS</sub> for 60 seconds. The MAX14434—MAX14436 family offers all three possible unidirectional channel configurations to accommodate any 4-channel design, including SPI, RS-232, RS-485, and digital I/O applications. Output enable for the A side of the MAX14435R/S/U/V is active low, making them ideal for isolating a port on a shared SPI bus since the CS signal can directly enable the MISO signal on the isolator. All other devices in the family have the traditional active-high enable. Devices are available with a maximum data rate of either 25Mbps or 200Mbps and with outputs that are either default-high or default-low. The default is the state the output assumes when the input is either not powered or is open-circuit. See the Ordering Information for suffixes associated with each option. Independent 1.71V to 5.5V supplies on each side of the isolator also make the devices suitable for use as level translators. The MAX14434—MAX14436 are available in a 16-pin widebody SOIC package with 8mm of creepage and clearance. The package material has a minimum comparative tracking index (CTI) of 600V, which gives it a group 1 rating in creepage tables. All devices are rated for operation at ambient temperatures of -40°C to +125°C.



## II. Manufacturing Information

A. Description/Function: Four-Channel, Fast, Low-Power,

5kV<sub>RMS</sub> Digital Isolators

B. Process: S18 C. Fabrication Location: USA D. Assembly Location: Taiwan

October 2, 2017 E. Date of Initial Production:

## III. Packaging Information

A. Package Type: 16-pin SOIC B. Lead Frame: Copper

C. Lead Finish: 100% matte Tin D. Die Attach: En4900g E. Bondwire: Au (1 mil dia.)

F. Mold Material: Epoxy with silica filler

G. Assembly Diagram: #05-100422 H. Flammability Rating: Class UL94-V0

I. Classification of Moisture Sensitivity per

JEDEC standard J-STD-020-C

Level 3

J. Single Layer Theta Ja: N/A°C/W N/A°C/W K. Single Layer Theta Jc: L. Multi Layer Theta Ja: 71°C/W M. Multi Layer Theta Jc: 24°C/W

## IV. Die Information

A. Passivation: Si<sub>3</sub>N<sub>4</sub>/SiO<sub>2</sub> (Silicon nitride/ Silicon dioxide)

B. Interconnect: AI/0.5%Cu with Ti/TiN Barrier

C. Minimum Metal Width: 0.23 microns (as drawn) D. Minimum Metal Spacing: 0.23 microns (as drawn)

E. Isolation Dielectric: SiO<sub>2</sub> F. Die Separation Method: Wafer Saw



#### V. Quality Assurance Information

A. Quality Assurance Contacts: Eric Wright (Reliability Engineering)

Brian Standley (Manager, Reliability) Bryan Preeshl (Vice President of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.

0.1% for all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm</li>D. Sampling Plan: Mil-Std-105D

## VI. Reliability Evaluation

### A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (\(\lambda\)) is calculated as follows:

$$\lambda = 1$$
MTTF

= 1.83 (Chi square value for MTTF upper limit)

(where  $4240 = \text{Temperature Acceleration factor assuming an act$ 

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

 $\lambda = 0.88 \times 10^{-9}$  $\lambda = 0.88 \text{ F.I.T. (60\% confidence level @ 25°C)}$ 

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S18 Process results in a FIT Rate of 0.05@ 25C and 0.93@ 55C (0.8 eV, 60% UCL)

### B. E.S.D. and Latch-Up Testing

The RV56-2 die type has been found to have all pins able to withstand an HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA and overvoltage per JEDEC JESD78.



# **Table 1**Reliability Evaluation Test Results

## MAX14436FAWE+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note	Ta = 135C Biased Time = 1000 hrs.	DC Parameters & functionality	240	0	

Note 1: Life Test Data may represent plastic DIP qualification lots.