RELIABILITY REPORT

FOR

MAX1324ECM+

PLASTIC ENCAPSULATED DEVICES

August 3, 2009

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Approved by
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Conclusion

The MAX1324ECM+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim"s continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim"s quality and reliability standards.

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I. Device Description

A. General

The MAX1316-MAX1318/MAX1320-MAX1322/MAX1324-MAX1326 14-bit, analog-to-digital converters (ADCs) offer two, four, or eight independent input channels. Independent track/hold (T/H) circuitry provides simultaneous sampling for each channel. The MAX1316/MAX1317/MAX1318 have a 0 to +5V input range with ±6.0V fault-tolerant inputs. The MAX1320/MAX1321/MAX1322 have a ±5V input range with ±16.5V fault-tolerant inputs. The MAX1324/MAX1325/MAX1326 have a ±10V input range with ±16.5V fault-tolerant inputs. These ADCs convert two channels in 2µs, and up to eight channels in 3.8µs, and have an 8-channel throughput of 250ksps per channel. Other features include a 10MHz T/H input bandwidth, internal clock, internal (+2.5V) or external (+2.0V to +3.0V) reference, and power-saving modes. A 16.6MHz, 14-bit, bidirectional, parallel interface provides the conversion results and accepts digital configuration inputs. These devices operate from a +4.75V to +5.25V analog supply and a separate +2.7V to +5.25V digital supply, and consume less than 50mA total supply current. These devices come in a 48-pin TQFP package and operate over the extended -40°C to +85°C temperature range.

II. Manufacturing Information

A. Description/Function:	8-/4-/2-Channel, 14-Bit, Simultaneous-Sampling ADCs with ±10V, ±5V, and 0 to +5V Analog Input Ranges
B. Process:	C6Y
C. Number of Device Transistors:	38612
D. Fabrication Location:	Japan
E. Assembly Location:	Malaysia
F. Date of Initial Production:	July 23, 2004

III. Packaging Information

A. Package Type:	48-pin LQFP
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-0578
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Multi Layer Theta Ja:	44°C/W
K. Multi Layer Theta Jc:	10°C/W

IV. Die Information

A. Dimensions:	203 X 210 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.6 microns (as drawn)
F. Minimum Metal Spacing:	0.6 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Ken Wendel (Director, Reliability Engineering) Bryan Preeshl (Managing Director of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 48 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 22.4 \times 10^{-9}$

$\lambda = 22.4$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly 1000 hour life test monitors on its processes. This data is published in the Product Reliability Report found at http://www.maxim-ic.com/. Current monitor data for the C6Y Process results in a FIT Rate of 0.82 @ 25C and 14.21 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

The industry standard 85°C/85%RH or HAST testing is monitored per device process once a quarter.

C. E.S.D. and Latch-Up Testing

The AC45-2 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2000 V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250 mA, 1.5x VCCMax Overvoltage per JESD78.

Table 1
Reliability Evaluation Test Results

MAX1324ECM+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	48	0
Moisture Testing (Note 2)				
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data