

RELIABILITY REPORT
FOR
MAX13204EALT+T
PLASTIC ENCAPSULATED DEVICES

April 18, 2014

MAXIM INTEGRATED

160 RIO ROBLES
SAN JOSE, CA 95134

Approved by
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Quality Assurance
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Conclusion

The MAX13204EALT+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX13202E/MAX13204E/MAX13206E/MAX13208E low-capacitance $\pm 30\text{kV}$ ESD-protection diode arrays are designed to protect sensitive electronics attached to communication lines. Each channel consists of a pair of diodes that steer ESD current pulses to VCC or GND. The MAX13202E/MAX13204E/MAX13206E/MAX13208E protect against ESD pulses up to $\pm 15\text{kV}$ Human Body Model (HBM) and $\pm 30\text{kV}$ Air-Gap Discharge, as specified in IEC 61000-4-2. These devices have a 6pF on-capacitance per channel, making them ideal for use on high-speed data I/O interfaces. The MAX13204E is a quad-ESD structure designed for Ethernet and FireWire® applications. The MAX13202E/MAX13206E/MAX13208E are 2-channel, 6-channel, and 8-channel devices. They are designed for cellphone connectors and SVGA video connections. These devices are available in 6-, 8-, and 10-pin μDFN packages and are specified over the -40°C to $+125^\circ\text{C}$ automotive operating temperature range.

II. Manufacturing Information

A. Description/Function:	2-/4-/6-/8-Channel $\pm 30\text{kV}$ ESD Protectors in μDFN
B. Process:	BCD8
C. Number of Device Transistors:	
D. Fabrication Location:	Oregon
E. Assembly Location:	Thailand
F. Date of Initial Production:	December 22, 2005

III. Packaging Information

A. Package Type:	6-pin μDFN
B. Lead Frame:	Substrate
C. Lead Finish:	Gold
D. Die Attach:	Non-conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-1978
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	N/A°C/W
K. Single Layer Theta Jc:	N/A°C/W
L. Multi Layer Theta Ja:	223.6°C/W
M. Multi Layer Theta Jc:	122.1°C/W

IV. Die Information

A. Dimensions:	43X35 mils
B. Passivation:	$\text{Si}_3\text{N}_4/\text{SiO}_2$ (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	3.0 microns (as drawn)
F. Minimum Metal Spacing:	3.0 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

- A. Quality Assurance Contacts: Don Lipps (Manager, Reliability Engineering)
Bryan Preeshl (Vice President of QA)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% for all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 48 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 22.9 \times 10^{-9}$$

$$\lambda = 22.9 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at <http://www.maximintegrated.com/qa/reliability/monitor>. Cumulative monitor data for the BCD8 Process results in a FIT Rate of 0.14 @ 25C and 2.34 @ 55C (0.8 eV, 60% UCL).

B. E.S.D. and Latch-Up Testing (lot NZO0AQ001C, D/C 0530)

The RU13 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA.

Table 1
Reliability Evaluation Test Results

MAX13204EALT+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	48	0	NZO0AQ001C, D/C 0530

Note 1: Life Test Data may represent plastic DIP qualification lots.