RELIABILITY REPORT

FOR

MAX13047EEVB+T / MAX13047EETA+T

PLASTIC ENCAPSULATED DEVICES

April 30, 2012

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

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Conclusion

The MAX13047EEVB+T / MAX13047EETA+T successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX13046E/MAX13047E ±15kV ESD-protected bidirectional level translators provide level shifting for data transfer in a multivoltage system. The MAX13046E is a single-channel translator, and the MAX13047E is a dual-channel translator. Externally applied voltages, VCC and VL, set the logic level on either side of the device. The MAX13046E/MAX13047E utilize a transmission-gate-based design to allow data translation in either direction (V L ⇔ VCC) on any single data line. The MAX13046E/MAX13047E accept VL from +1.1V to the minimum of either +3.6V or (VCC + 0.3V), and V CC from +1.65V to +5.5V, making these devices ideal for data transfer between low-voltage ASICs/PLDs and higher voltage systems. The MAX13046E/MAX13047E feature a shutdown mode that reduces supply current to less than 1µA thermal short-circuit protection, and ±15kV ESD protection on the VCC side for enhanced protection in applications that route signals externally. The MAX13046E/MAX13047E operate at a guaranteed data rate of 8Mbps when push-pull driving is used. The MAX13046E is available in a 6-pin µDFN package, and the MAX13047E is available in a 10-pin UTQFN. Both devices are specified over the extended -40°C to +85°C operating temperature range.

II. Manufacturing Information

A. Description/Function:	Single- and Dual-Channel, Bidirectional Low-Level Translators	
B. Process:	S45	
C. Number of Device Transistors:	618	
D. Fabrication Location:	USA or Japan	
E. Assembly Location:	Thailand	China, Malaysia, Taiwan and Thailand
F. Date of Initial Production:	July 26, 2008	

III. Packaging Information

A. Package Type:	10-pin ultra QFN	8-pin TDFN 2x2
B. Lead Frame:	Copper	Copper
C. Lead Finish:	NiPdAu	100% matte Tin
D. Die Attach:	Non-conductive	Conductive
E. Bondwire:	Au (1 mil dia.)	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-3102	#05-9000-3025
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1	Level 1
J. Single Layer Theta Ja:	°C/W	110°C/W
K. Single Layer Theta Jc:	°C/W	37°C/W
L. Multi Layer Theta Ja:	143.2°C/W	83.9°C/W
M. Multi Layer Theta Jc:	20.1°C/W	37°C/W

IV. Die Information

A. Dimensions:	30 X 30 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1 = 0.5 / Metal2 = 0.6 / Metal3 = 0.6 microns (as drawn)
F. Minimum Metal Spacing:	Metal1 = 0.45 / Metal2 = 0.5 / Metal3 = 0.6 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Richard Aburano (Manager, Reliability Engineering) Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 48 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 22.9 \times 10^{-9}$

$\lambda = 22.9$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maxim-ic.com/qa/reliability/monitor. Cumulative monitor data for the S45 Process results in a FIT Rate of 0.06 @ 25C and 1.00 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot TJPZBQ001E, D/C 0817)

The LT10 die type has been found to have all pins able to withstand a HBM transient pulse of +/- 2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/- 250mA and overvoltage per JEDEC JESD78.

Table 1

Reliability Evaluation Test Results

MAX13047EEVB+T / MAX13047EETA+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135C Biased Time = 192 hrs.	DC Parameters & functionality	48	0	TJPZBQ001D, D/C 0818

Note 1: Life Test Data may represent plastic DIP qualification lots.