

RELIABILITY REPORT
FOR
MAX13013EEBX+
(MAX13013/MAX13014/MAX3023)
CHIP SCALE PACKAGE

February 20, 2009

MAXIM INTEGRATED PRODUCTS

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Conclusion

The MAX13013EEBX+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I.Device Description	V.Quality Assurance Information
II.Manufacturing Information	VI.Reliability Evaluation
III.Packaging Information	IV.Die Information
.....Attachments	

I. Device Description

A. General

The MAX13013/MAX13014/MAX3023 single-/dual-/quadlevel translators provide the level shifting necessary to allow 100Mbps data transfer in a multivoltage system. Externally applied voltages, VCC and VL, set the logic levels on either side of the device. Logic signals present on the VL side of the device appear as a higher voltage logic signal on the VCC side of the device, and viceversa. The MAX13013 single-, the MAX13014 dual-, and the MAX3023 (UCSP™ package) quad-level translators feature an enable (EN) input. The MAX3023 (TSSOP package) quad-level translator features EN and EN inputs. When disabled, each device places all inputs/outputs on both sides in tri-state and reduces the VCC supply current to 0.03μA, and the VL supply current to 0.1μA. These devices operate at a guaranteed 100Mbps data rate for VL > 1.8V. The MAX13013/MAX13014/MAX3023 accept a +1.65V to +3.6V VCC voltage and a +1.2V to (VCC - 0.4V) VL voltage, making them ideal for data transfer between low-voltage ASICs/programmable logic devices (PLDs) and higher voltage systems. The MAX13013 is available in 3 x 2 UCSP and 6-pin SC70 packages. The MAX13014 is available in 3 x 3 UCSP and 8-pin SOT23 packages. The MAX3023 is available in 4 x 3 UCSP and 14-pin TSSOP packages. All devices operate over the extended -40°C to +85°C temperature range.

II. Manufacturing Information

A. Description/Function:	+1.2V to +3.6V, 0.1 μ A, 100Mbps, Single-/Dual-/Quad-Level Translators
B. Process:	S4
C. Number of Device Transistors:	
D. Fabrication Location:	Texas
E. Assembly Location:	Dallas
F. Date of Initial Production:	April 24, 2004

III. Packaging Information

A. Package Type:	9-pin UCSP
B. Lead Frame:	N/A
C. Lead Finish:	N/A
D. Die Attach:	N/A
E. Bondwire:	N/A
F. Mold Material:	N/A
G. Assembly Diagram:	#
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1

IV. Die Information

A. Dimensions:	61 X 61 mils
B. Passivation:	Si ₃ N ₄ /SiO ₂ (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1 = 0.5 / Metal2 = 0.6 / Metal3 = 0.6 microns (as drawn)
F. Minimum Metal Spacing:	Metal1 = 0.45 / Metal2 = 0.5 / Metal3 = 0.6 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO ₂
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

- A. Quality Assurance Contacts: Ken Wendel (Director, Reliability Engineering)
Bryan Preeshl (Managing Director of QA)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 48 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 22.4 \times 10^{-9}$$

$\lambda = 22.4$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly 1000 hour life test monitors on its processes. This data is published in the Product Reliability Report found at <http://www.maxim-ic.com/>. Current monitor data for the S4 Process results in a FIT Rate of 4.6 @ 25C and 79.2 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

The industry standard 85°C/85%RH or HAST testing is monitored per device process once a quarter.

C. E.S.D. and Latch-Up Testing

The RT62 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2500 V per Mil-Std 883 Method 3015.7. Latch-Up testing has shown that this device withstands a current of +/-250 mA.

Table 1
Reliability Evaluation Test Results

MAX13013EEBX+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	48	0
Moisture Testing (Note 2) 85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2 & 3) Temperature Cycle	-40°C/125°C 1000 Cycles (Note 3)	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic Package/Process data

Note 3: Ramp rate 11°C/minute, dwell=15 minutes, One cycle/hour.